Quad Protected High-Side MOSFET Driver

FEATURES

- Fully Enhances N-Channel MOSFET Switches
- **8V to 48V Power Supply Range**
- **Protected from –15V to 60V Supply Transients**
- **Individual Short-Circuit Protection**
- **Individual Automatic Restart Timers**
- Programmable Current Limit, Delay Time, and Auto-Restart Period
- Voltage-Limited Gate Drive
- Defaults to OFF State with Open Input
- Flowthrough Input to Output Pinout
- Available in 20-Lead DIP or SOL Package

APPLICATIONS

- Industrial Control
- Avionics Systems
- Automotive Switches
- Stepper Motor and DC Motor Control
- Electronic Circuit Breaker

DESCRIPTION

The LT1161 is a quad high-side gate driver allowing the use of low cost N-channel power MOSFETs for high-side switching applications. It has four independent switch channels, each containing a completely self-contained charge pump to fully enhance an N-channel MOSFET switch with no external components.

Also included in each switch channel is a drain sense comparator that is used to sense switch current. When a preset current level is exceeded, the switch is turned off. The switch remains off for a period of time set by an external timing capacitor and then automatically attempts to restart. If the fault is still present, this cycle repeats until the fault is removed, thus protecting the MOSFET.

The LT1161 has been specifically designed for harsh operating environments such as industrial, avionics, and automotive applications where poor supply regulation and/or transients may be present. The device will not sustain damage from supply voltages of –15V to 60V.

TYPICAL APPLICATION

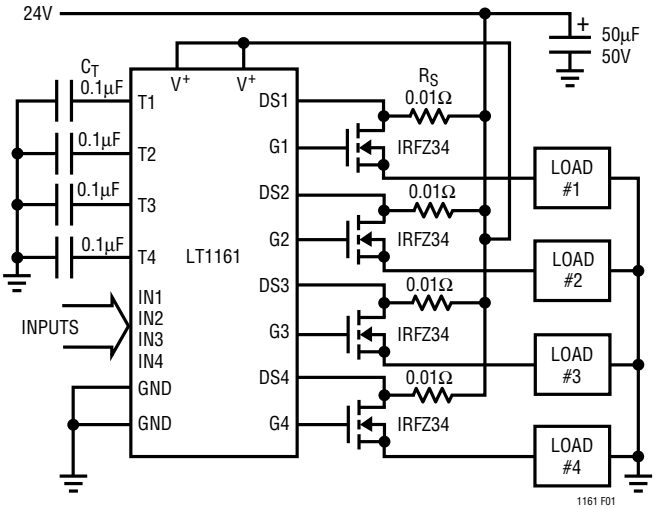
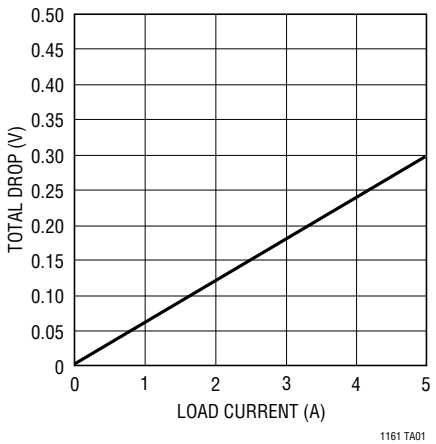


Figure 1. Protected Quad High-Side Switch

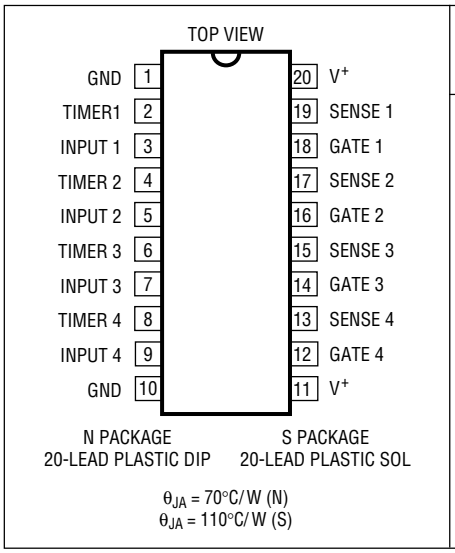
Switch Drop vs Load Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltages (Pins 11, 20) ..... –15V to 60V
Input Voltages (Pins 3, 5, 7, 9) ..... (GND – 0.3V) to 15V
Gate Voltages (Pins 12, 14, 16, 18) 75V
Sense Voltages (Pins 13, 15, 17, 19) ..... $V^+ \pm 5V$
Current (Any Pin) 50mA
Operating Temperature Range
LT1161C ..... 0°C to 70°C
LT1161I ..... – 40°C to 85°C
Junction Temperature Range (Note 1)
LT1161C ..... 0°C to 125°C
LT1161I ..... – 40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1161CN
LT1161CS
LT1161IN
LT1161IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V^+ = 12V to 48V each channel, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Supply Current	All Channels OFF (Note 2)		3	4.5	6.5	mA
$\Delta I_{S(ON)}$	Delta Supply Current (ON State)	Measure Increase in I_S per Channel			1	1.35	mA
V_{INH}	Input High Voltage		●	2			V
V_{INL}	Input Low Voltage		●			0.8	V
I_{IN}	Input Current	V_{IN} = 2V V_{IN} = 5V	● ●	15 55	30 110	50 185	µA µA
C_{IN}	Input Capacitance				5		pF
$V_{T(TH)}$	Timer Threshold Voltage	V_{IN} = 2V, Adjust V_T	●	2.7	3	3.3	V
$V_{T(CL)}$	Timer Clamp Voltage	V_{IN} = 0.8V		3.2	3.5	3.8	V
I_T	Timer Charge Current	$V_{IN} = V_T$ = 2V		9	14	20	µA
V_{SEN}	Drain Sense Threshold Voltage Temperature Coefficient			50	65 +0.33	80	mV %/°C
I_{SEN}	Drain Sense Input Current	V^+ = 48V, V_{SEN} = 65mV			0.5	1.5	µA
$V_{GATE} – V^+$	Gate Voltage Above Supply	V^+ = 8V V^+ = 12V V^+ = 24V V^+ = 48V	 ● ● ●	4 7 10 10	4.5 8.5 12 12	6 10 14 14	V V V V
t_{ON}	Turn-ON Time	V^+ = 24V, V_{GATE} > 32V, C_{GATE} = 1000pF		100	220	400	µs
t_{OFF}	Turn-OFF Time	V^+ = 24V, V_{GATE} < 2V, C_{GATE} = 1000pF			75	200	µs
$t_{OFF(CL)}$	Current Limit Turn-OFF Time	V^+ = 24V, ($V^+ – V_{SENSE}$) → 0.1V, C_{GATE} = 1000pF			25	50	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

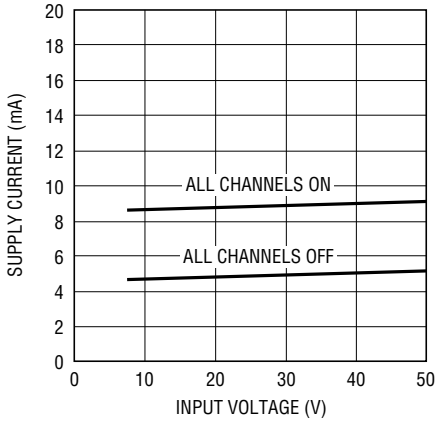
LT1161CN, LT1161IN: $T_J = T_A + (P_D \times 70°C/W)$

LT1161CS, LT1161IS: $T_J = T_A + (P_D \times 110°C/W)$

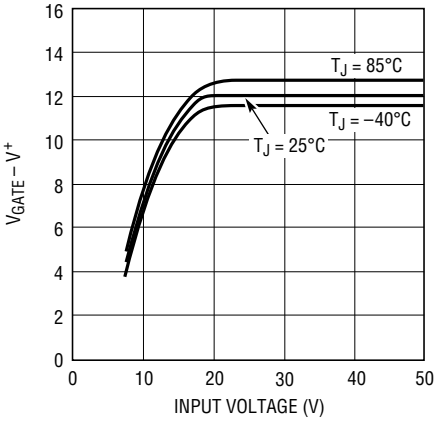
Note 2: Both V^+ pins (11, 20) must be connected together and both ground pins (1, 10) must be connected together.

TYPICAL PERFORMANCE CHARACTERISTICS

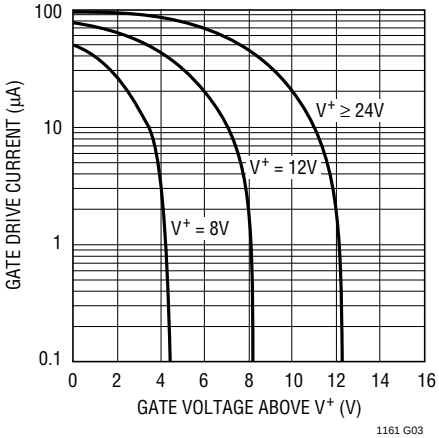
Supply Current



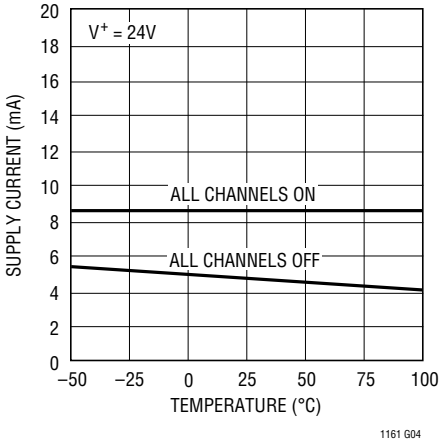
MOSFET Gate Voltage Above V+



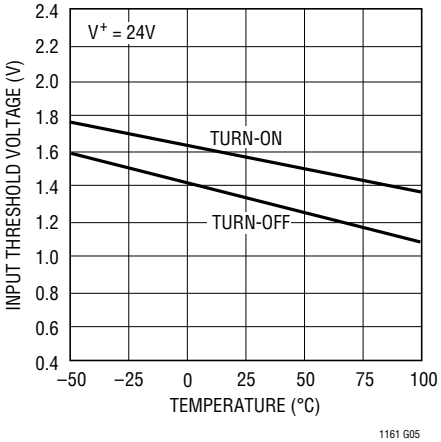
MOSFET Gate Drive Current



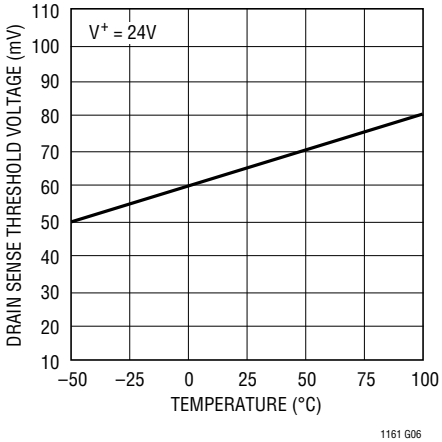
Supply Current



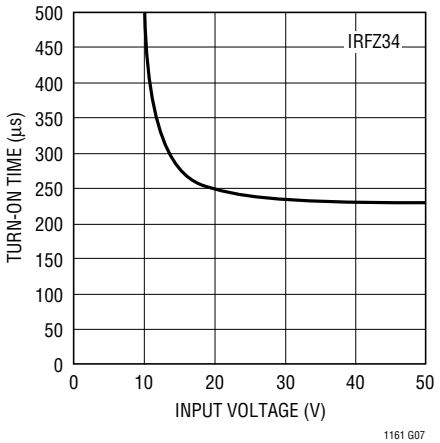
Input Threshold Voltage



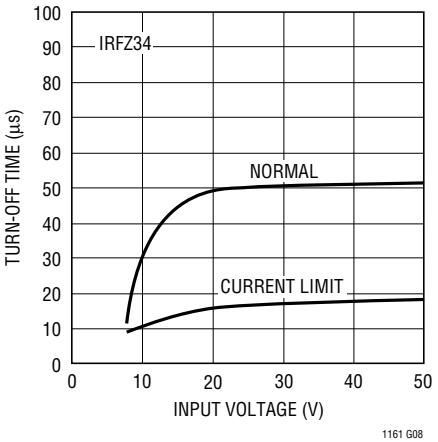
Drain Sense Threshold Voltage



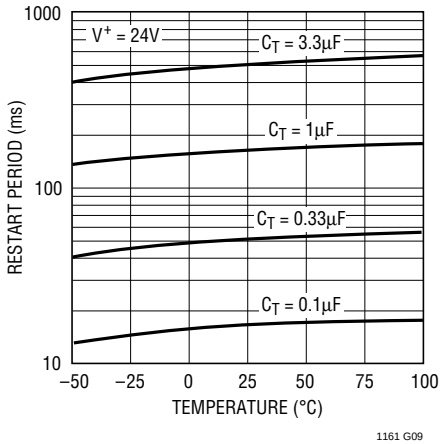
Turn-ON Time Driving MOSFET



Turn-OFF Time Driving MOSFET



Automatic Restart Period



PIN FUNCTIONS

Supply Pins: The two supply pins are internally connected and must also be externally connected. In addition to providing the operating current for the LT1161, the supply pins also serve as the Kelvin connection for the current sense comparators. The supply pins must be connected to the positive side of the drain sense resistors for proper operation of the current sense.

Input Pins: The input pins are active high and each pin activates a separate internal charge pump when switched ON. The input threshold is TTL/CMOS compatible but may be taken as high as 15V with or without the supply powered. Each input has approximately 200mV of hysteresis and an internal 75k pull-down resistor.

Gate Pins: The gate pins drive the power MOSFET gates. When an input is ON, the corresponding gate pin is pumped approximately 12V above the supply. These pins have a relatively high impedance when above the rail (the equivalent of a few hundred kilohms). Care should be taken to minimize any loading by parasitic resistance to ground or supply.

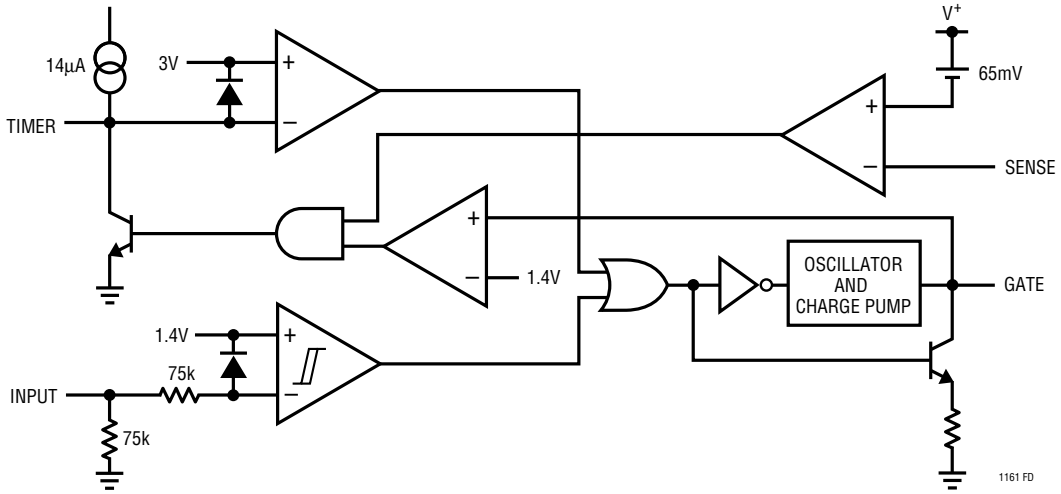
Sense Pins: Each sense pin connects to the input of a supply-referenced comparator with a 65mV nominal offset. When a sense pin is taken more than 65mV below supply, the MOSFET gate for that channel is driven low and the corresponding timing capacitor discharged. Each current-sense comparator operates completely independently. The 65mV typical threshold has a +0.33%/°C temperature coefficient, which closely matches the TC of drain sense resistors formed from copper PC traces.

Some loads require high in-rush currents. An RC time delay can be added between the drain sense resistor and the sense pin to ensure that the current-sense comparator does not false trigger during start-up (see Applications Information). However, a maximum of 10kΩ can be inserted between a drain sense resistor and the sense pin. If current sense is not required in any channel, the sense pin for that channel is tied to supply.

Timer Pins: A timing capacitor C_T from each timer pin to ground sets the restart time following overcurrent detection. C_T is rapidly discharged to less than 1V and then recharged by a 14μA nominal current source back to the timer threshold, whereupon restart is attempted. If current sense is not required in any channel, the timer pin for that channel is left open.

Ground Pins: The two ground pins are internally connected and must also be externally connected.

FUNCTIONAL DIAGRAM (Each Channel)



OPERATION (Each Channel, Refer to Functional Diagram)

The LT1161 gate pin has two states, OFF and ON. In the OFF state it is held low, while in the ON state it is pumped to 12V above supply by a self-contained 750kHz charge pump. The OFF state is activated when either the input pin is below 1.4V or the timer pin is below 3V. Conversely, for the ON state to be activated, both the input and timer pins must be above their thresholds.

If left open, the input pin is held low by a 75k resistor, while the timer pin is held a diode drop above 3V by a 14μA pull-up current source. Thus the timer pin automatically reverts to the ON state, subject to the input also being high. The input has approximately 200mV of hysteresis.

The sense pin normally connects to the drain of the power MOSFET, which returns through a low valued drain sense resistor to supply. When the gate is ON and the MOSFET drain current exceeds the level required to generate a 65mV drop across the drain sense resistor, the sense comparator activates a pull-down NPN which rapidly pulls the timer pin below 3V. This in turn causes the timer comparator to override the input pin and activate the gate pin OFF state, thus protecting the power MOSFET. In order for the sense comparator to accurately sense MOSFET drain current, the LT1161 supply pins must be connected directly to the positive side of the drain sense resistors.

When the MOSFET gate voltage is less than 1.4V, the timer pin is released. The 14μA current source then slowly charges the timing capacitor back to 3V where the charge pump again starts to drive the gate pin high. If a fault still exists, such as a short circuit, the sense comparator threshold will again be exceeded and the timer cycle will repeat until the fault is removed (see Figure 2).

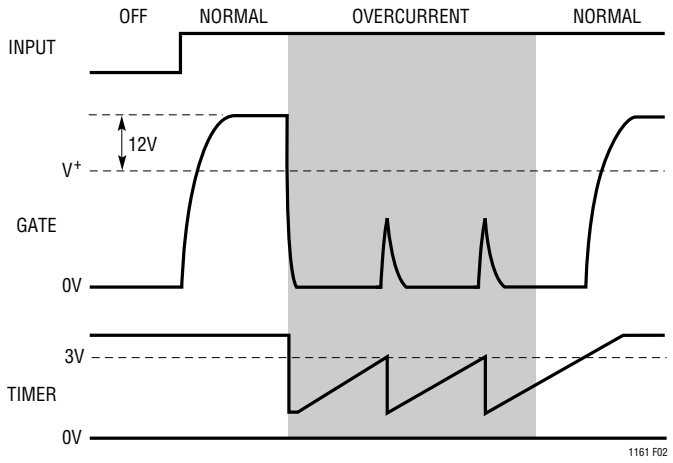


Figure 2. Timing Diagram

APPLICATIONS INFORMATION

Input/Supply Sequencing

There are no input/supply sequencing requirements for the LT1161. The input may be taken up to 15V with the supply at 0V. When the supply is turned on with an input high, the MOSFET turn-on will be inhibited until the timing capacitor charges to 3V (i.e., for one restart cycle). The two V+ pins (11, 20) must always be connected to each other.

Isolating the Inputs

Operation in harsh environments may require isolation to prevent ground transients from damaging control logic. The LT1161 easily interfaces to low cost opto-isolators. The network shown in Figure 3 ensures that the input will be pulled above 2V, but not exceed the absolute maximum rating, for supply voltages of 12V to 48V over the entire temperature range. In order to maintain the OFF state, the opto must have less than 20μA of dark current (leakage) hot.

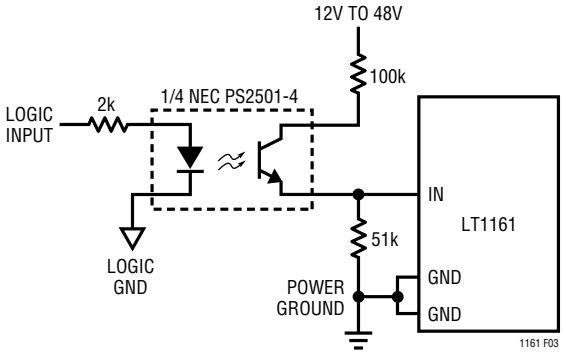


Figure 3. Isolating the Inputs

APPLICATIONS INFORMATION

Drain Sense Configuration

The LT1161 uses supply-referenced current sensing. One input of each channel's current-sense comparator is connected to a drain sense pin, while the second input is offset 65mV below the supply bus inside the device. For this reason, pins 11 and 20 of the LT1161 must be treated not only as supply pins, but as the reference inputs for the current-sense comparators.

Figure 4 shows the proper drain sense configuration for the LT1161. Note that the sense pin goes to the drain end of the sense resistor, while the two V^+ pins are tied to each other and connected to supply at the same point as the positive ends of the sense resistors. Local supply decoupling at the LT1161 is important at high input voltages (see Protecting Against Supply Transients).

The drain sense threshold voltage has a positive temperature coefficient, allowing PTC sense resistors to be used (see Printed Circuit Board Shunts). The selection of R_S should be based on the minimum threshold voltage:

$$R_S = \frac{50mV}{I_{SET}}$$

Thus the 0.02Ω drain sense resistor in Figure 4 would yield a minimum trip current of 2.5A. This simple configuration is appropriate for resistive or inductive loads which do not generate large current transients at turn-on.

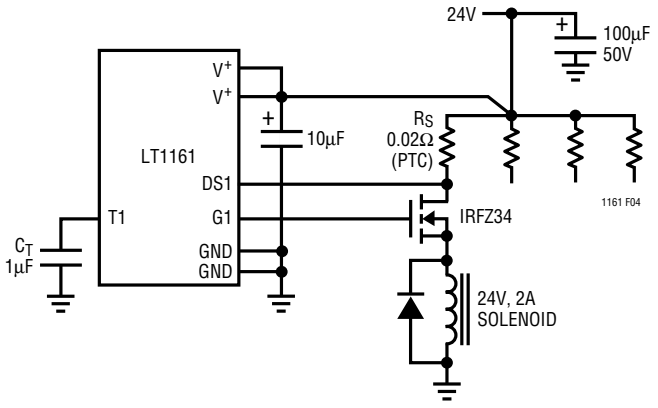


Figure 4. Drain Sense Configuration

Automatic Restart Period

The timing capacitor C_T shown in Figure 4 determines the length of time the power MOSFET is held off following a current limit trip. Curves are given in the Typical Performance Characteristics to show the restart period for various values of C_T. For example, C_T = 0.33µF yields a 50ms restart period.

Defeating Automatic Restart

Some applications are required to remain off after a fault occurs. When the LT1161 is being driven from CMOS logic, this can be easily implemented by connecting resistor R1 between the input and timer pins as shown in Figure 5. R1 supplies the sustaining current for an SCR which latches the timer pin low. This prevents the MOSFET gate from turning ON until the input has been recycled.

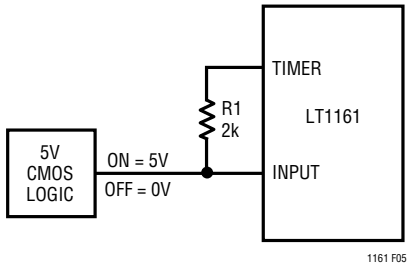


Figure 5. Latch-Off Input Network (Auto-Restart Defeated)

Inductive vs Capacitive Loads

Turning on an inductive load produces a relatively benign ramp in MOSFET current. However, when an inductive load is turned off, the current stored in the inductor needs somewhere to decay. A clamp diode connected directly across each inductive load normally serves this purpose. If a diode is not employed the LT1161 clamps the MOSFET gate 0.7V below ground. This causes the MOSFET to resume conduction during the current decay with (V^+ + V_{GS} + 0.7V) across it, resulting in high dissipation peaks.

Capacitive loads exhibit the opposite behavior. Any load that includes a decoupling capacitor will generate a current equal to $C_{LOAD} \times (\partial V/\partial t)$ during capacitor in-rush. With large electrolytic capacitors, the resulting current

APPLICATIONS INFORMATION

spike can play havoc with the power supply and false trip the current-sense comparator.

Turn-on ∂V/∂t is controlled by the addition of the simple network shown in Figure 6. This network takes advantage of the fact that the MOSFET acts as a source follower during turn-on. Thus the ∂V/∂t on the source can be controlled by controlling the ∂V/∂t on the gate:

$$\frac{\partial V}{\partial t} = \frac{V^+ - V_{TH}}{10^5 \times C1}$$

where V_{TH} is the MOSFET gate threshold voltage. Multiplying C_{LOAD} times this ∂V/∂t yields the value of the current spike. For example, if V^+ = 24V, V_{TH} = 2V, and C1 = 0.1µF, ∂V/∂t = 2.2V/ms, resulting in a 2.2A turn-on spike into 1000µF. The diode and second resistor in the network ensure fast current limit turn-off.

When turning off a capacitive load, the source of the MOSFET can "hang up" if the load resistance does not discharge C_{LOAD} as fast as the gate is being pulled down. If this is the case, a diode may have to be added from source to gate to prevent $V_{GS(MAX)}$ from being exceeded.

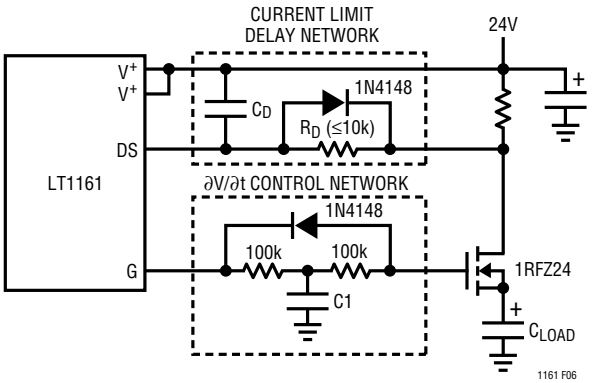


Figure 6. ∂V/∂t Control and Current Limit Delay

Adding Current Limit Delay

When capacitive loads are being switched or in very noisy environments, it is desirable to add delay in the drain current-sense path to prevent false tripping (inductive loads normally do not need delay). This is accomplished by the current limit delay network shown in Figure 6. R_D and C_D delay the overcurrent trip for drain currents up to approximately $10 \times I_{SET}$, above which the diode conducts and provides immediate turn-off (see Figure 7). *To ensure proper operation of the timer, C_D must be ≤ C_T.*

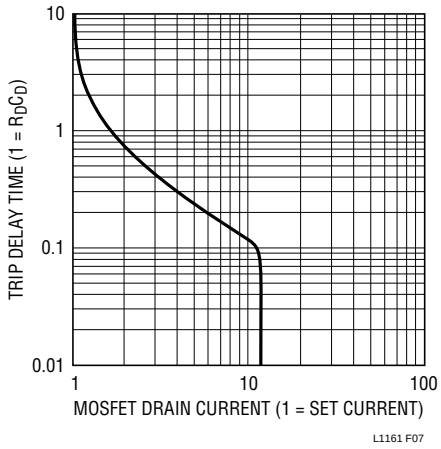


Figure 7. Current Limit Delay Time

Printed Circuit Board Shunts

The sheet resistance of 1oz. copper clad is approximately $5 \times 10^{-4}\Omega$/square with a temperature coefficient of +0.39%/°C. Since the LT1161 drain sense threshold has a similar temperature coefficient (+0.33%/°C), this offers the possibility of nearly zero TC current sensing using "free" drain sense resistors made out of PC trace material.

A conservative approach is to use 0.02" of width for each 1A of current for 1oz. copper. Combining the LT1161 drain sense threshold with the 1oz. copper sheet resistance results in a simple expression for width and length:

Width (1oz. Cu) = 0.02" × I_{SET}

Length (1oz. Cu) = 2"

The width for 2oz. copper would be halved while the length would remain the same.

Bends may be incorporated into the resistor to reduce space; each bend is equivalent to approximately 0.6 × width of straight length. Kelvin connections should be employed by running separate traces from the ends of the resistors back to the LT1161 V^+ and sense pins. See Application Note 53 for further information on printed circuit board shunts.

APPLICATIONS INFORMATION

Low Voltage/Wide Supply Range Operation

When the supply is <12V, the LT1161 charge pumps do not produce sufficient gate voltage to fully enhance standard N-channel MOSFETs. For these applications, logic-level MOSFETs can be used to extend operation down to 8V. If the MOSFET has a maximum V_{GS} rating of 15V or greater, then it can also be used up to the 60V (absolute maximum) rating of the LT1161. MOSFETs are available from both Motorola and Siliconix which meet these criteria.

Protecting Against Supply Transients

The LT1161 is 100% tested and guaranteed to be safe from damage with 60V applied between the V^+ and ground pins. However, when this voltage is exceeded, even for a few microseconds, the result can be a catastrophic failure. For this reason *it is imperative that the LT1161 not be exposed to supply transients above 60V*.

For proper current-sense operation, the V^+ pins are required to be connected to the positive side of the drain sense resistors (see Drain Sense Configuration). Therefore, the best way to prevent supply transients is to ensure that the supply is adequately decoupled at the point where the V^+ pins and drain sense resistors meet. Several hundred microfarads may be required with high current switches.

When operating voltages approach the 60V absolute maximum rating of the LT1161, local supply decoupling between the V^+ pins (11, 20) and ground pins (1, 10) is highly recommended. A small ferrite bead between the supply connection and local capacitor can also be effective in suppressing transients. Note however, that resistance should not be added in series with the V^+ pins because it will cause an error in the current sense threshold.

Fault Feedback

Two methods can be used to derive switch status. First, the timer pin voltage can be monitored to indicate when the switch is turned off due to current limit. During normal operation (ON or OFF), the timer voltage is 3.5V and only during current limit does the voltage drop below 3V.

The second method shown in Figure 8 uses a quad exclusive-NOR gate to indicate when the output of the switch has not obeyed the input command (i.e., output low when it should be high or vice versa). In addition to current limit, this gives a fault indication if the switch is shorted or if the load is open.

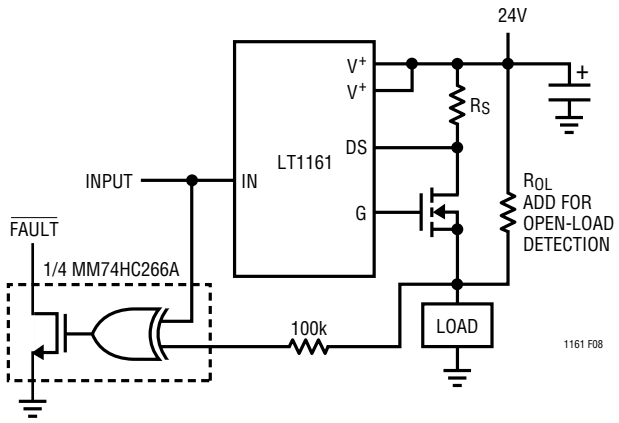


Figure 8. Fault Feedback Using Exclusive-NOR Gate

Low-Side Driving

Although the LT1161 is primarily targeted at high-side (grounded load) switch applications, it can also be used for low-side (supply-connected load), or mixed high- and low-side switch applications. Figures 9a and 9b illustrate LT1161 switch channels driving low-side power MOSFETs. Because the LT1161 charge pump tries to pump the gate of the N-channel MOSFET *above* supply, a clamp zener is required to prevent the V_{GS} (absolute maximum) of the MOSFET from being exceeded. The LT1161 gate drive is current limited for this purpose so that no resistance is needed between the gate pin and zener.

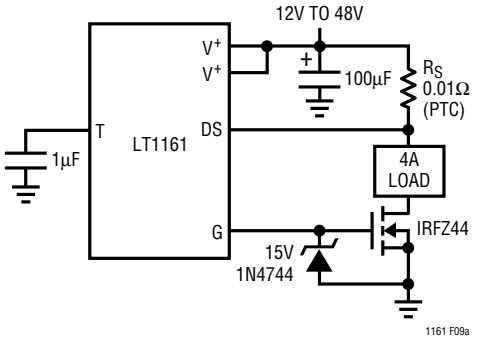


Figure 9a. Low-Side Driver with Load Current Sensing

APPLICATIONS INFORMATION

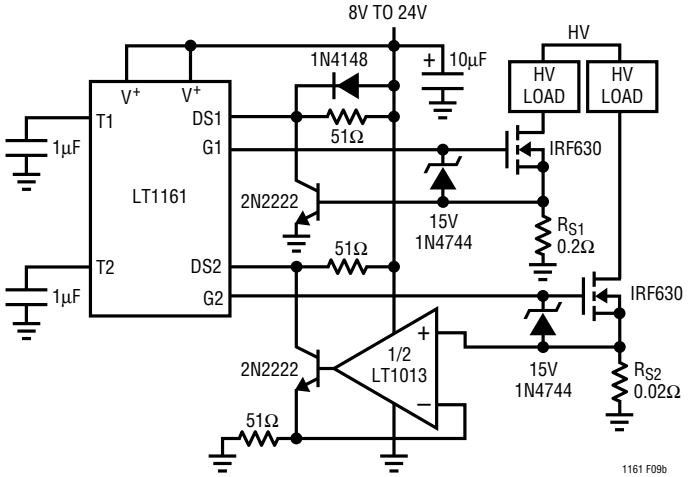


Figure 9b. Low-Side Drivers with Two Approaches for Source Current Sensing

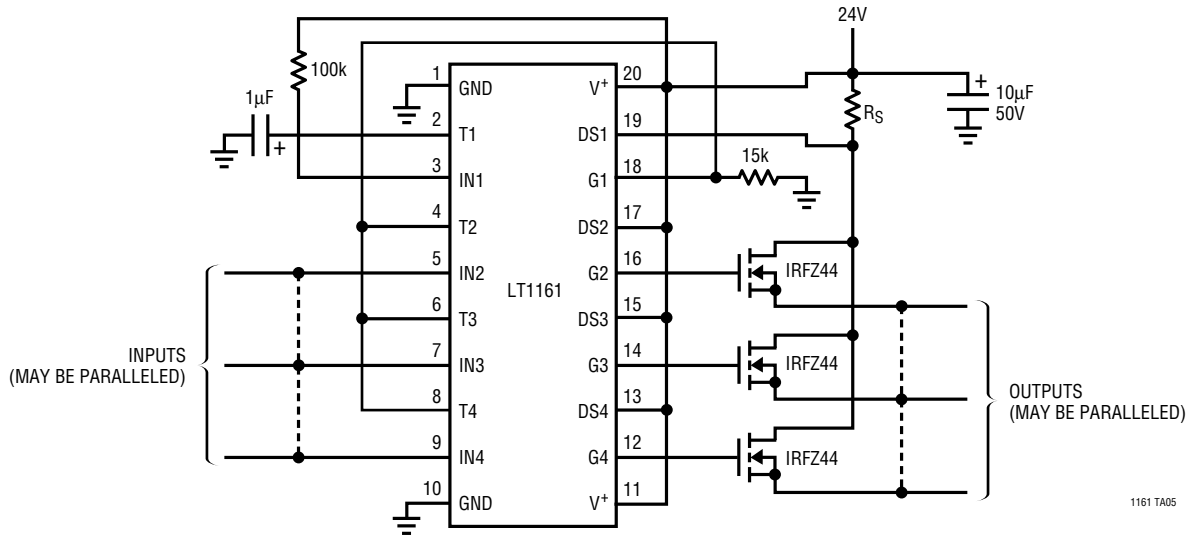
Current sensing for protecting low-side drivers can be done in several different ways. In the Figure 9a circuit, the supply voltage for the load is assumed to be within the supply operating range of the LT1161. This allows the load to be returned to supply through current-sense resistor R_S, providing normal operation of the LT1161 protection circuitry.

If the load cannot be returned to supply through R_S, or the load supply voltage is higher than the LT1161 supply, the current sense must be moved to the source of the low-side MOSFET. Figure 9b shows two approaches to source sensing. On channel 1, current limit occurs when the voltage across sense resistor R_{S1} thresholds the V_{BE} of the NPN transistor, causing the LT1161 drain sense pin to be pulled down.

The channel 2 circuit of Figure 9b uses an operational amplifier (must common mode to ground) to level shift the voltage across R_{S2} up to the drain sense pin. This approach allows the use of a much smaller sense resistor which could be made from PC trace material. In both cases, the LT1161 restart timers function the same as in high-side switch applications.

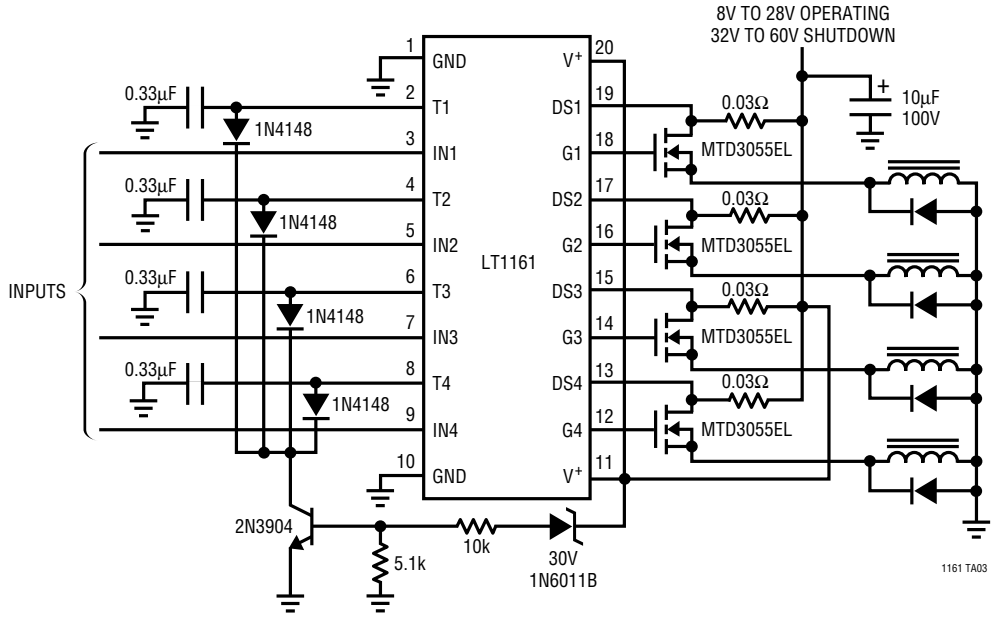
TYPICAL APPLICATIONS

Using an Extra Channel to Do Common Current Limit for Multiple/Paralleled Switches

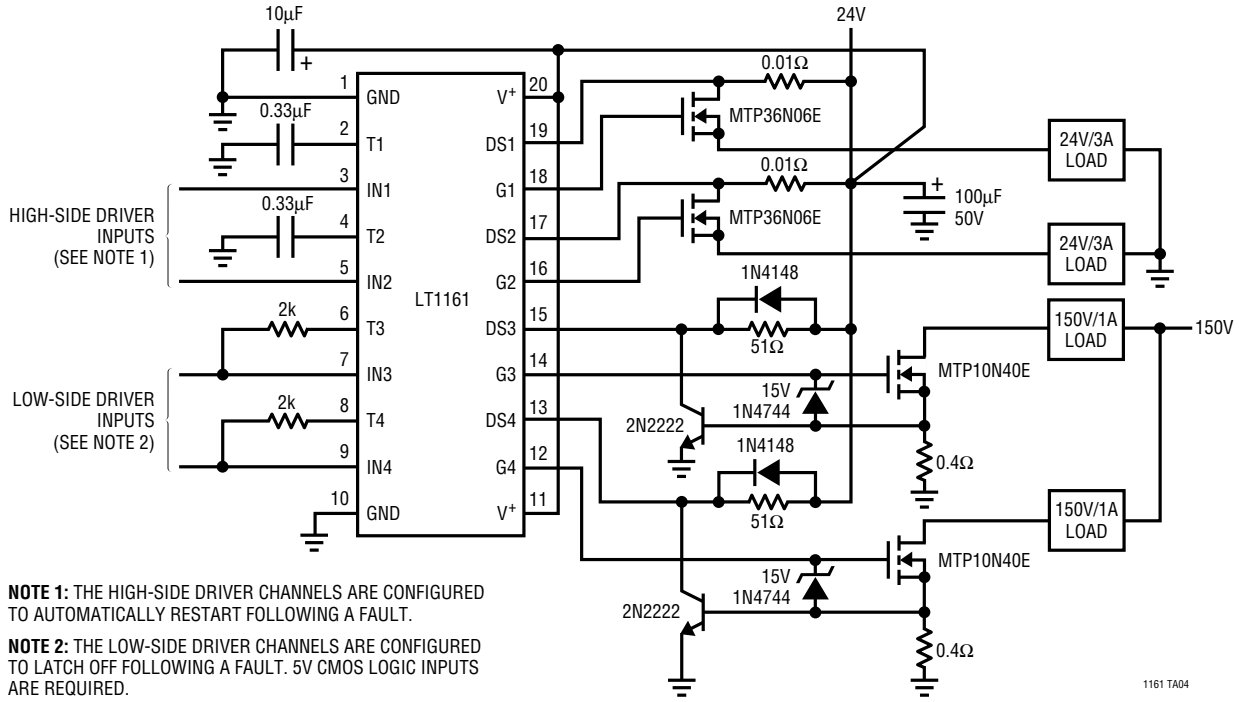


TYPICAL APPLICATIONS

Protected Quad 1A Automotive Solenoid Driver with Overvoltage Shutdown



Protected Quad Switch with Mixed Low- and High-Side Driving

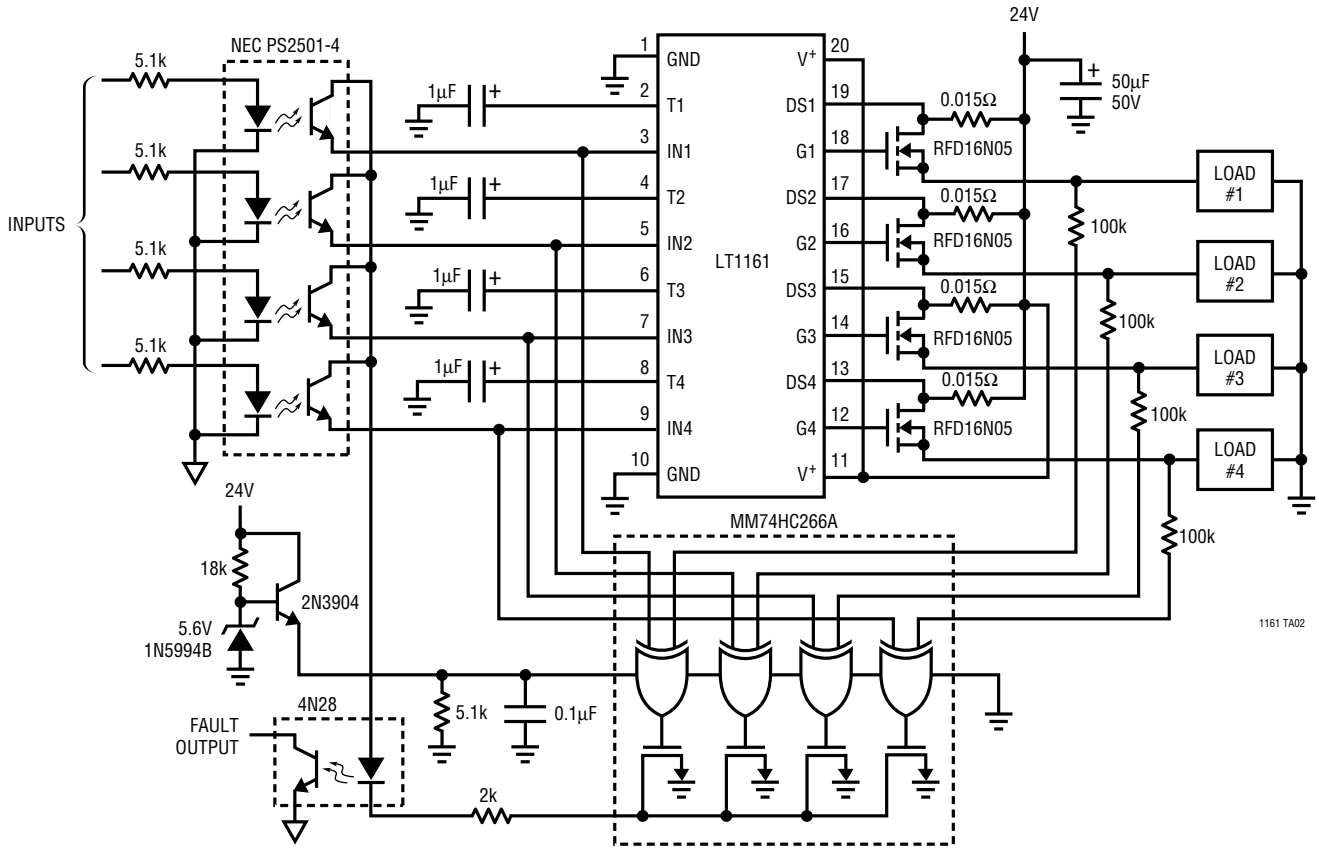


NOTE 1: THE HIGH-SIDE DRIVER CHANNELS ARE CONFIGURED TO AUTOMATICALLY RESTART FOLLOWING A FAULT.

NOTE 2: THE LOW-SIDE DRIVER CHANNELS ARE CONFIGURED TO LATCH OFF FOLLOWING A FAULT. 5V CMOS LOGIC INPUTS ARE REQUIRED.

TYPICAL APPLICATIONS

Protected Quad 2A Industrial Switch with Isolated Inputs and Fault Output

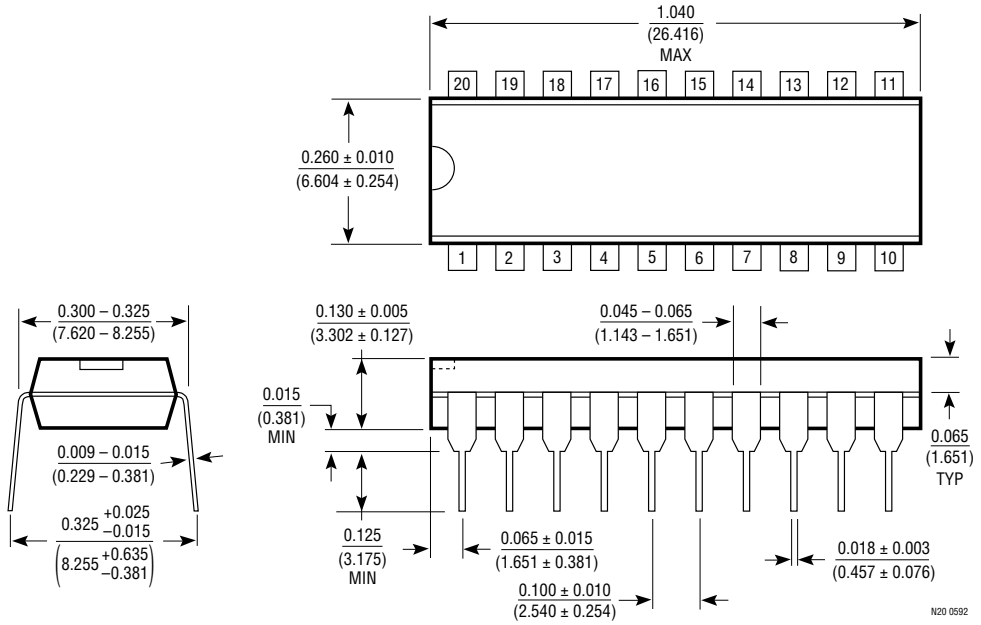


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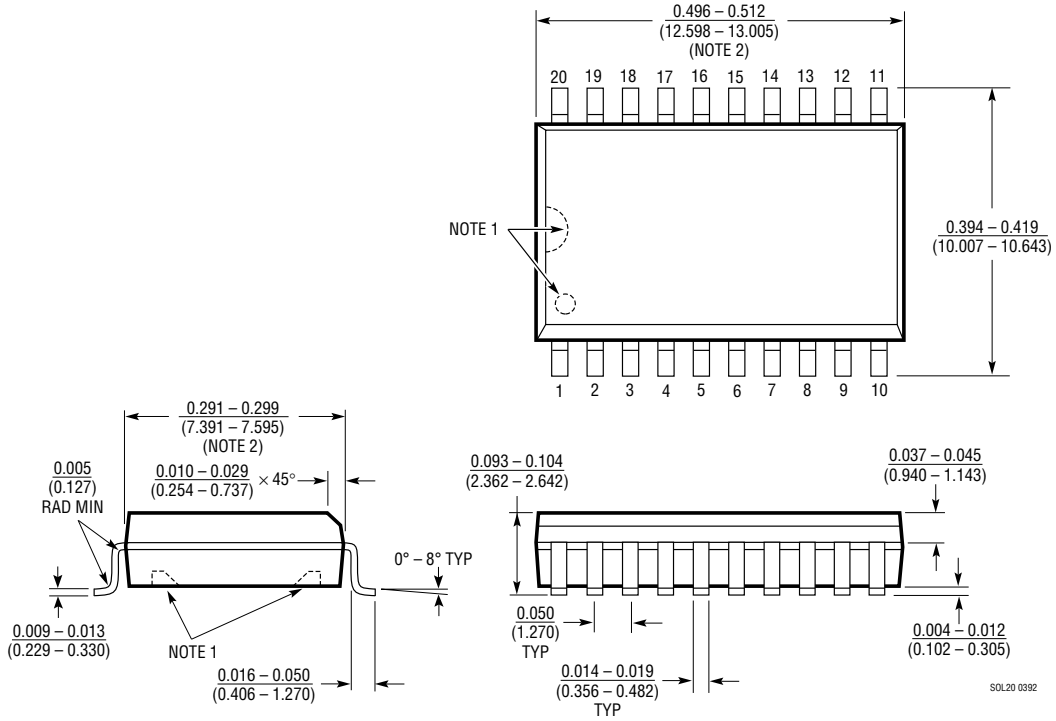
PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

N Package
20-Lead Plastic DIP



S Package
20-Lead Plastic SOL



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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