Precision, High Speed, JFET Input Operational Amplifiers

FEATURES

- *Guaranteed* Offset Voltage 150µV Max
  –55°C to 125°C 500µV Max
- *Guaranteed* Drift 4µV/°C Max
- *Guaranteed* Bias Current
  70°C 150pA Max
  125°C 2.5nA Max
- *Guaranteed* Slew Rate 12V/µs Min

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters
- Fast, Precision Sample-and-Hold

DESCRIPTION

The LT1055/LT1056 JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/µs slew rate and 6.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 50µV, 1.2µV/°C drift, bias currents of 40pA at 70°C and 500pA at 125°C.

The 150µV maximum offset voltage specification is the best available on any JFET input operational amplifier.

The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

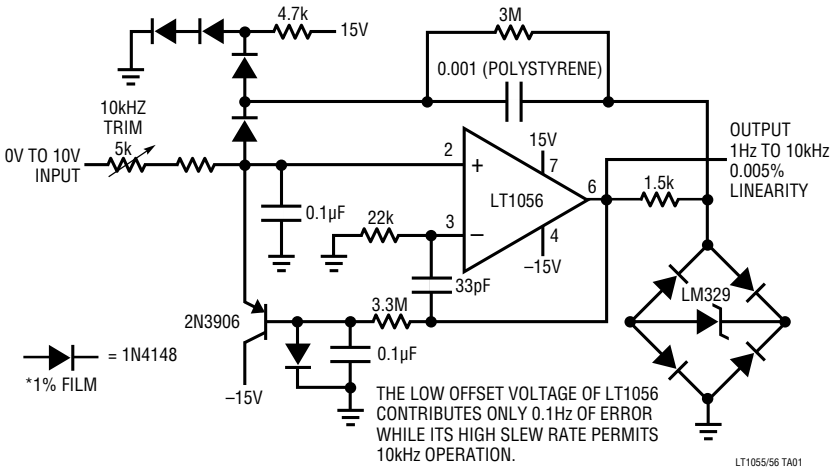
The voltage-to-frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/LT1056.

For a JFET input op amp with 23V/µs guaranteed slew rate, refer to the LT1022 data sheet.

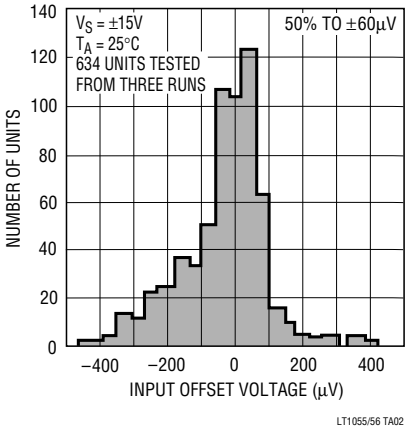
LT and LTC are registered trademarks and LT is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

0kHz to 10kHz Voltage-to-Frequency Converter



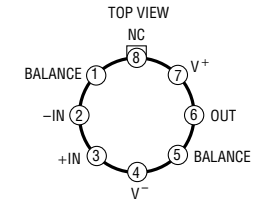
Distribution of Input Offset Voltage (H Package)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
LT1055AM/LT1055M/LT1056AM/
LT1056M ..... –55°C to 125°C
LT1055AC/LT1055C/LT1056AC/
LT1056C ..... 0°C to 70°C
Storage Temperature Range
All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

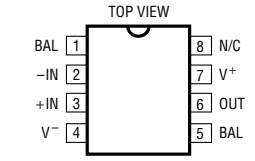
PACKAGE/ORDER INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN
T_{JMAX} = 150°C, θ_{JA} = 150°C/W, θ_{JC} = 45°C/W

ORDER PART NUMBER

LT1055ACH LT1056ACH
LT1055CH LT1056CH
LT1055AMH LT1056AMH
LT1055MH LT1056MH



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 100°C, θ_{JA} = 130°C/W

LT1055CN8
LT1056CN8

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM/LT1056AM LT1055AC/LT1056AC MIN	TYP	MAX	LT1055M/LT1056M LT1055CH/LT1056CH LT1055CN8/LT1056CN8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note1)	LT1055 H Package	—	50	150	—	70	400	µV
		LT1056 H Package	—	50	180	—	70	450	µV
		LT1055 N8 Package	—	—	—	—	120	700	µV
		LT1056 N8 Package	—	—	—	—	140	800	µV
I_{OS}	Input Offset Current	Fully Warmed Up	—	2	10	—	2	20	pA
I_B	Input Bias Current	Fully Warmed Up	—	±10	±50	—	±10	±50	pA
		V_{CM} = 10V	—	30	130	—	30	150	pA
	Input Resistance: Differential		—	10^{12}	—	—	10^{12}	—	Ω
	Common Mode	V_{CM} = –11V to 8V	—	10^{12}	—	—	10^{12}	—	Ω
		V_{CM} = 8V to 11V	—	10^{11}	—	—	10^{11}	—	Ω
	Input Capacitance		—	4	—	—	4	—	pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1055	—	1.8	—	—	2.0	—	μV_{P-P}
		LT1056	—	2.5	—	—	2.8	—	μV_{P-P}
	Input Noise Voltage Density	f_0 = 10Hz (Note 2)	—	28	50	—	30	60	$nV/\sqrt{Hz}$
		f_0 = 1kHz (Note 3)	—	14	20	—	15	22	$nV/\sqrt{Hz}$
I_n	Input Noise Current Density	f_0 = 10Hz, 1kHz (Note 4)	—	1.8	4	—	1.8	4	$fA/\sqrt{Hz}$
A_{VOL}	Large-Signal Voltage Gain	V_0 = ±10V R_L = 2k	150	400	—	120	400	—	V/mV
		R_L = 1k	130	300	—	100	300	—	V/mV
	Input Voltage Range		±11	±12	—	±11	±12	—	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±11V	86	100	—	83	98	—	dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±18V	90	106	—	88	104	—	dB
V_{OUT}	Output Voltage Swing	R_L = 2k	±12	±13.2	—	±12	±13.2	—	V
SR	Slew Rate	LT1055	10	13	—	7.5	12	—	V/µs
		LT1056	12	16	—	9.0	14	—	V/µs
GBW	Gain-Bandwidth Product	f = 1MHz LT1055	—	5.0	—	—	4.5	—	MHz
		LT1056	—	6.5	—	—	5.5	—	MHz
I_S	Supply Current	LT1055	—	2.8	4.0	—	2.8	4.0	mA
		LT1056	—	5.0	6.5	—	5.0	7.0	mA
	Offset Voltage Adjustment Range	R_{POT} = 100k	—	±5	—	—	±5	—	mV

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AC LT1056AC MIN	LT1055AC LT1056AC TYP	LT1055AC LT1056AC MAX	LT1055CH/LT1056CH LT1055CN8/LT1056CN8 MIN	LT1055CH/LT1056CH LT1055CN8/LT1056CN8 TYP	LT1055CH/LT1056CH LT1055CN8/LT1056CN8 MAX	UNITS
V_{OS}	Input Offset Voltage (Note1)	LT1055 H Package	●	—	100	330	—	140	750	µV
		LT1056 H Package	●	—	100	360	—	140	800	µV
		LT1055 N8 Package	●	—	—	—	—	250	1250	µV
		LT1056 N8 Package	●	—	—	—	—	280	1350	µV
	Average Temperature Coefficient of Input Offset Voltage	H Package (Note 5)	●	—	1.2	4.0	—	1.6	8.0	µV/°C
		N8 Package (Note 5)	●	—	—	—	—	3.0	12.0	µV/°C
I_{OS}	Input Offset Current	Warmed Up LT1055	●	—	10	50	—	16	80	pA
		$T_A = 70°C$ LT1056	●	—	14	70	—	18	100	pA
I_B	Input Bias Current	Warmed Up LT1055	●	—	±30	±150	—	±40	±200	pA
		$T_A = 70°C$ LT1056	●	—	±40	±80	—	±50	±240	pA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	80	250	—	60	250	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{Cm} = \pm 10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	89	105	—	87	103	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.1	—	±12	±13.1	—	V

$V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AM LT1056AM MIN	LT1055AM LT1056AM TYP	LT1055AM LT1056AM MAX	LT1055M LT1056M MIN	LT1055M LT1056M TYP	LT1055M LT1056M MAX	UNITS
V_{OS}	Input Offset Voltage (Note1)	LT1055	●	—	180	500	—	250	1200	µV
		LT1056	●	—	180	550	—	250	1250	µV
	Average Temperature Coefficient of Input Offset Voltage	(Note 5)	●	—	1.3	4.0	—	1.8	8.0	µV/°C
I_{OS}	Input Offset Current	Warmed Up LT1055	●	—	0.20	1.2	—	0.25	1.8	nA
		$T_A = 125°C$ LT1056	●	—	0.25	1.5	—	0.30	2.4	nA
I_B	Input Bias Current	Warmed Up LT1055	●	—	±0.4	±2.5	—	±0.5	±4.0	nA
		$T_A = 125°C$ LT1056	●	—	±0.5	±3.0	—	±0.6	±5.0	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120	—	35	120	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	88	104	—	86	102	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±12.9	—	±12	±12.9	—	V

The ● denotes specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power; (b) at $T_A = 25°C$ only, with the chip heated to approximately 38°C for the LT1055 and to 45°C for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 2: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

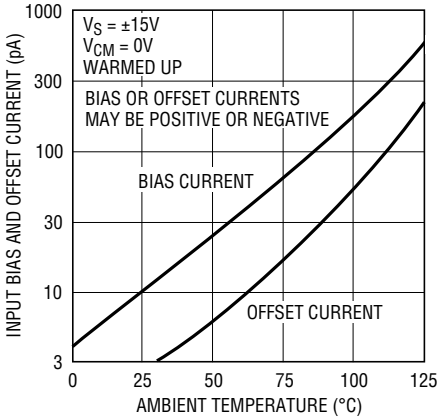
Note 3: This parameter is tested on a sample basis only.

Note 4: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

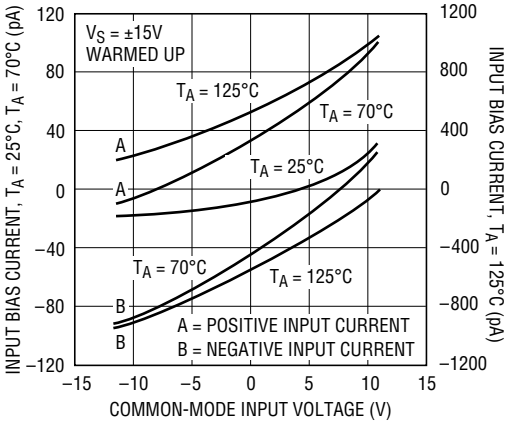
Note 5: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+. Devices tested to tighter drift specifications are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

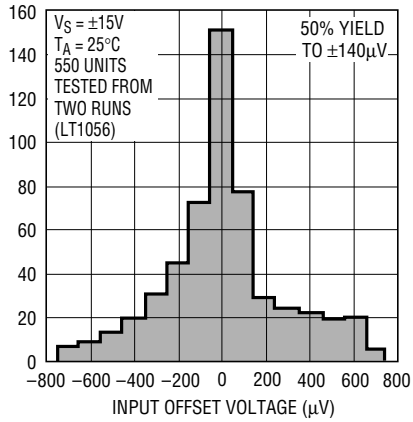
Input Bias and Offset Currents vs Temperature



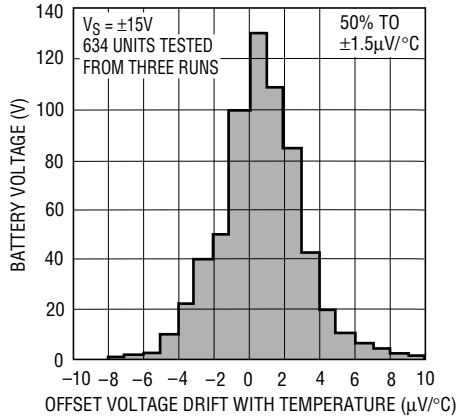
Input Bias Current Over the Common-Mode Range



Distribution of Input Offset Voltage (N8 Package)

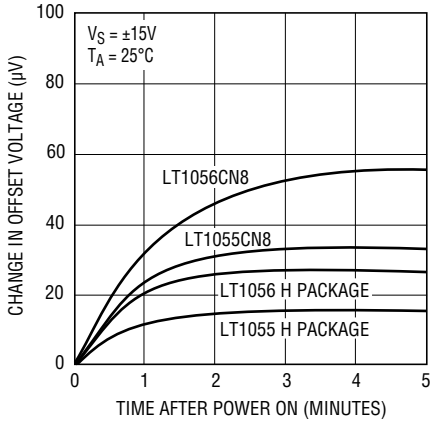


Distribution of Offset Voltage Drift with Temperature (H Package)*

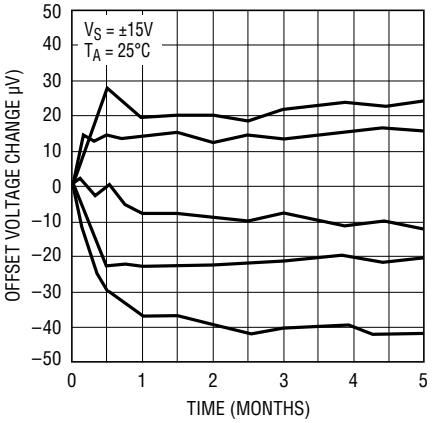


*DISTRIBUTION IN THE PLASTIC (N8) PACKAGE IS SIGNIFICANTLY WIDER.

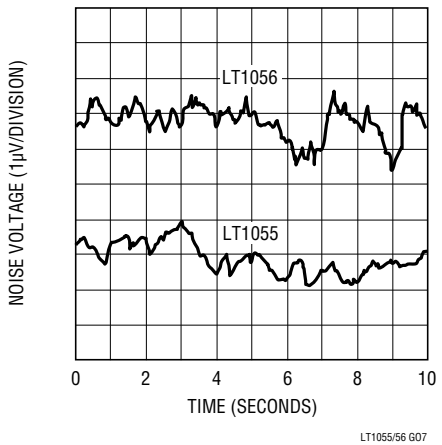
Warm-Up Drift



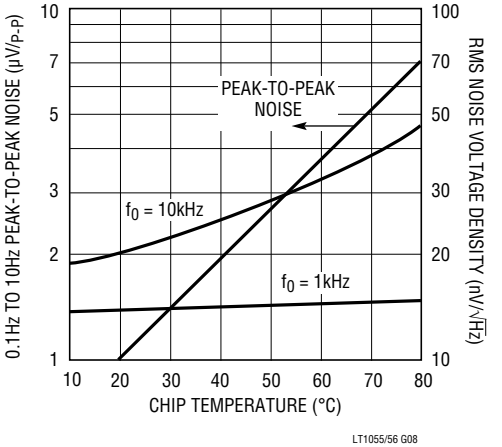
Long Term Drift of Representative Units



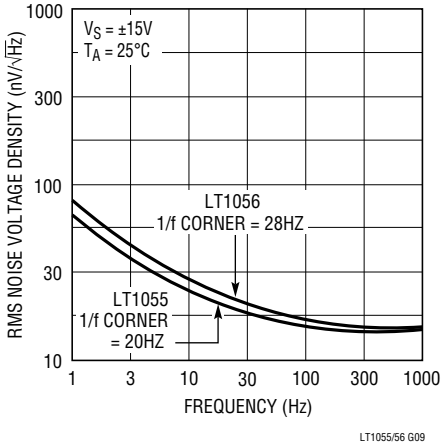
0.1Hz to 10Hz Noise



Noise vs Chip Temperature

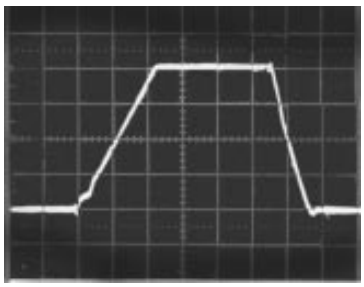


Voltage Noise vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

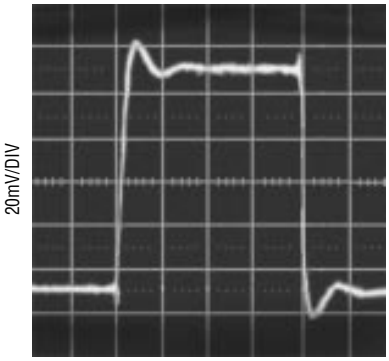
LT1056 Large-Signal Response



A_V = 1, C_L = 100pF, 0.5µs/DIV

LT1055/56 G10

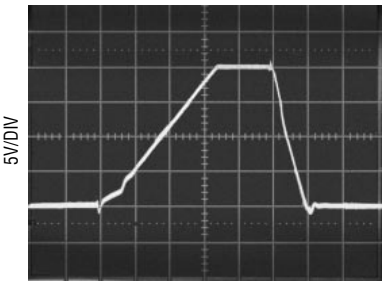
Small-Signal Response



A_V = 1, C_L = 100pF, 0.2µs/DIV

LT1055/56 G11

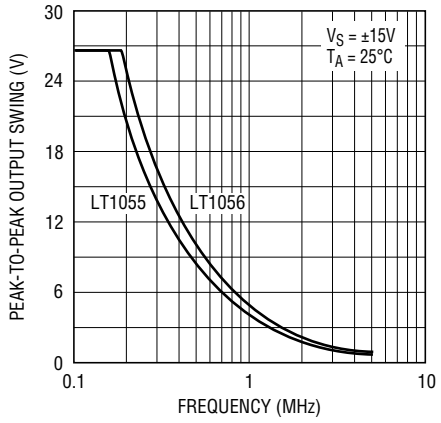
LT1055 Large-Signal Response



A_V = 1, C_L = 100pF, 0.5µs/DIV

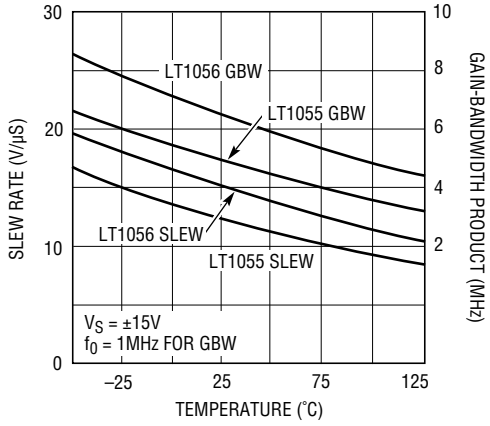
LT1055/56 G12

Undistorted Output Swing vs Frequency



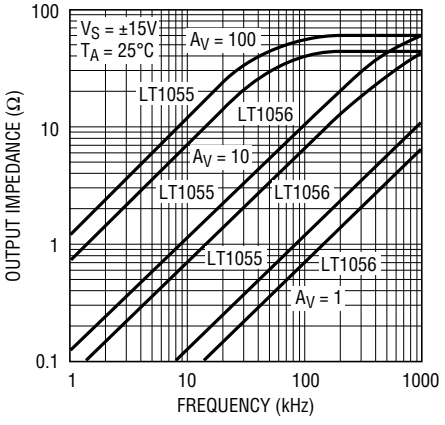
LT1055/56 G13

Slew Rate, Gain-Bandwidth vs Temperature



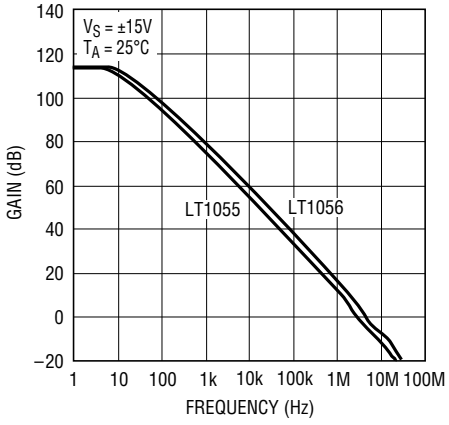
LT1055/56 G14

Output Impedence vs Frequency



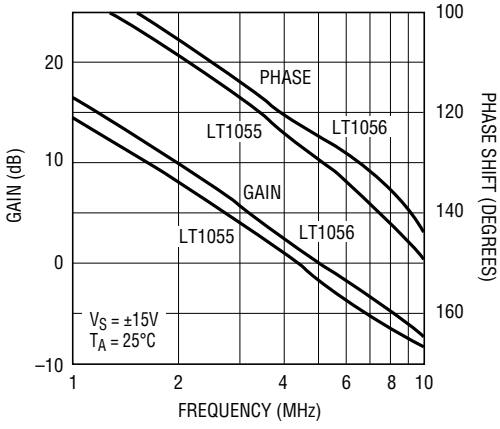
LT1055/56 G15

Gain vs Frequency



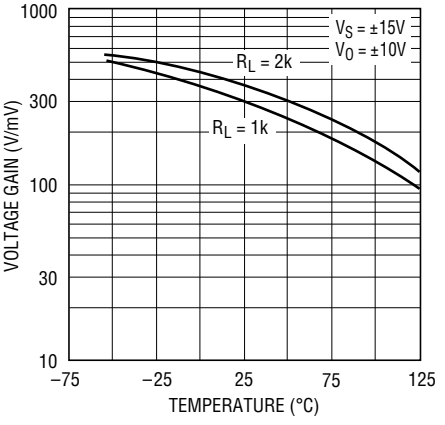
LT1055/56 G16

Gain, Phase Shift vs Frequency



LT1055/56 G17

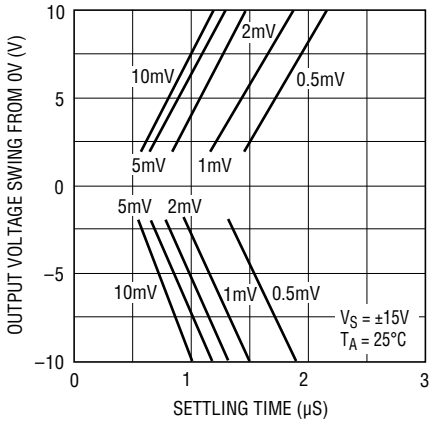
Voltage Gain vs Temperature



LT1055/56 G18

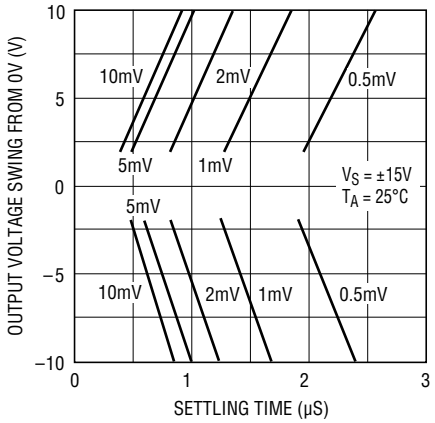
TYPICAL PERFORMANCE CHARACTERISTICS

LT1055 Settling Time



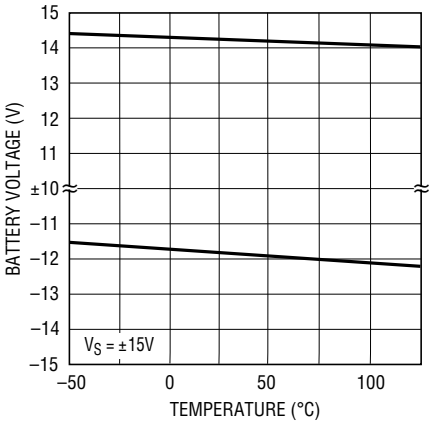
LT1055/56 G19

LT1056 Settling Time



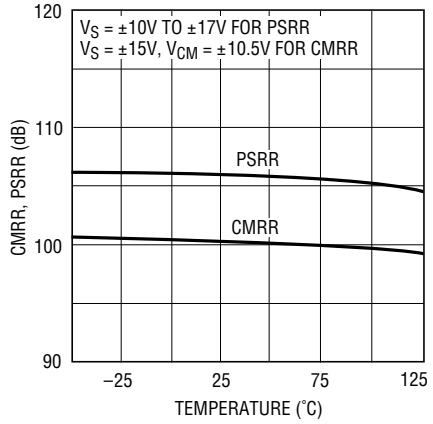
LT1055/56 G20

Common-Mode Range vs Temperature



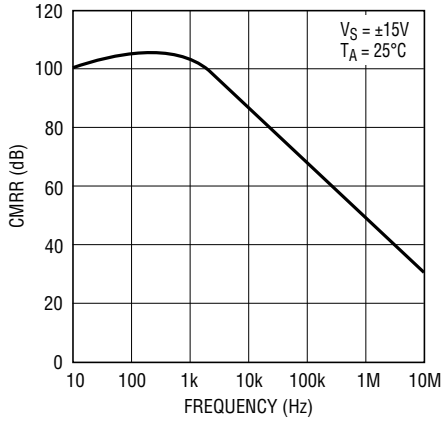
LT1055/56 G21

Common-Mode and Power Supply Rejections vs Temperature



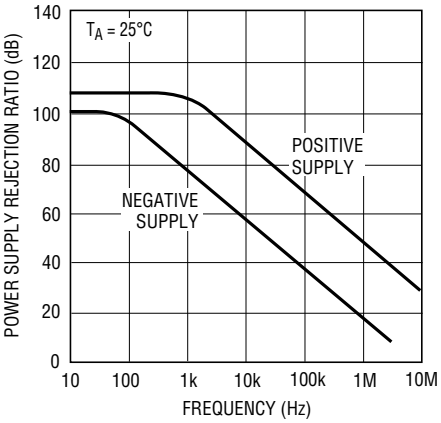
LT1055/56 G22

Common-Mode Rejection Ratio vs Frequency



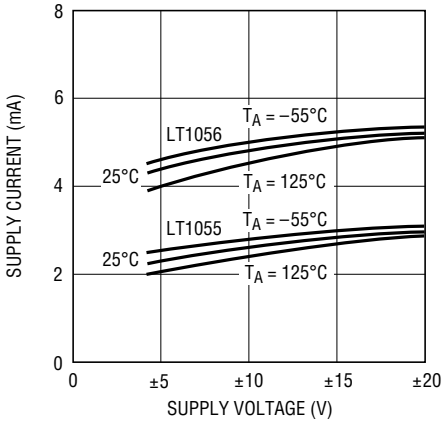
LT1055/56 G23

Power Supply Rejection Ratio vs Frequency



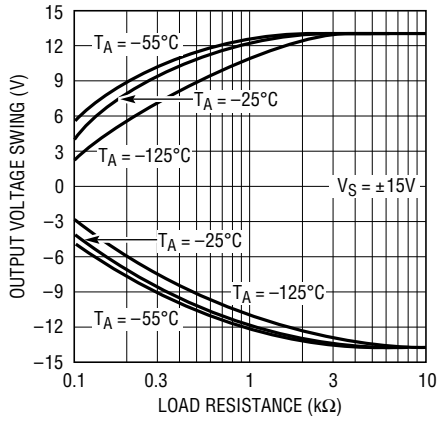
LT1055/56 G24

Supply Current vs Supply Voltage



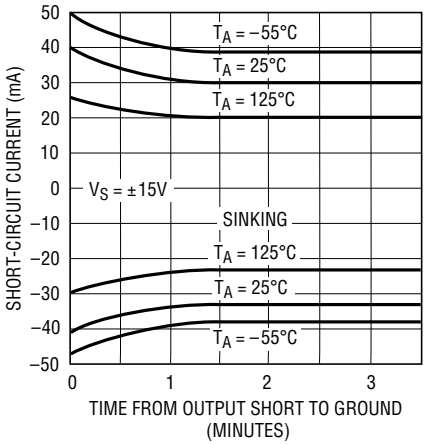
LT1055/56 G25

Output Swing vs Load Resistance



LT1055/56 G26

Short-Circuit Current vs Time

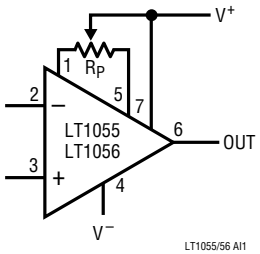


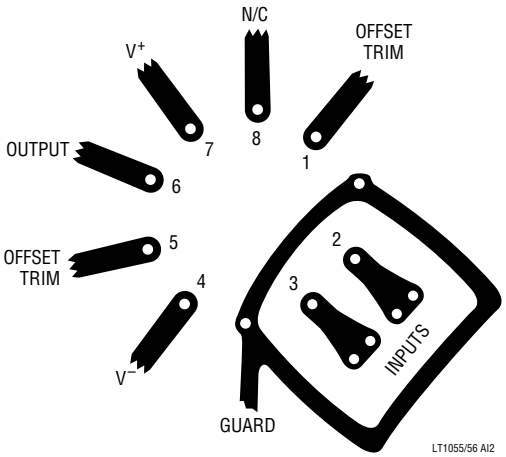
LT1055/56 G27

APPLICATIONS INFORMATION

The LT1055/LT1056 may be inserted directly into LF155A/LT355A, LF156A/LT356A, OP-15 and OP-16 sockets. Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the positive supply.

Offset Nulling





No appreciable change in offset voltage drift with temperature will occur when the device is nulled with a potentiometer, R_P, ranging from 10k to 200k.

The LT1055/LT1056 can also be used in LF351, LF411, AD547, AD611, OPA-111, and TL081 sockets, provided that the nulling cicuitry is removed. Because of the LT1055/LT1056's low offset voltage, nulling will not be necessary in most applications.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere-microvolt level accuracy of the LT1055/LT1056 proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in noninverting connnections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Teflon is a trademark of Dupont.

The LT1055/LT1056 has the lowest offset voltage of any JFET input op amp available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical 20μV hysteresis (30μV on the M grades) when cycled over the –55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than 10μV) hysteresis effect.

The offset voltage and drift performance are also affected by packaging. In the plastic N8 package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device matching and drift are degraded. Consequently, for best DC performance, as shown in the typical performance distribution plots, the TO-5 H package is recommended.

Noise Performance

The current noise of the LT1055/LT1056 is practically immeasurable at $1.8fA/\sqrt{Hz}$. At 25°C it is negligible up to 1G of source resistance, R_S (compound to the noise of R_S). Even at 125°C it is negligible to 100M of R_S.

APPLICATIONS INFORMATION

The voltage noise spectrum is characterized by a low 1/f corner in the 20Hz to 30Hz range, significantly lower than on other competitive JFET input op amps. Of particular interest is the fact that with any JFET IC amplifier, the frequency location of the 1/f corner is proportional to the square root of the internal gate leakage currents and, therefore, noise doubles every 20°C. Furthermore, as illustrated in the noise versus chip temperature curves, the 0.1Hz to 10Hz peak-to-peak noise is a strong function of temperature, while wideband noise (f_0 = 1kHz) is practically unaffected by temperature.

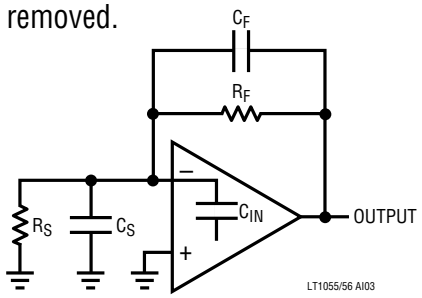
Consequently, for optimum low frequency noise, chip temperature should be minimized. For example, operating an LT1056 at ±5V supplies or with a 20°C/W case-to-ambient heat sink reduces 0.1Hz to 10Hz noise from typically 2.5μV_{P-P} (±15V, free-air) to 1.5μV_{P-P}. Similiarly, the noise of an LT1055 will be 1.8μV_{P-P} typically because of its lower power dissipation and chip temperature.

High Speed Operation

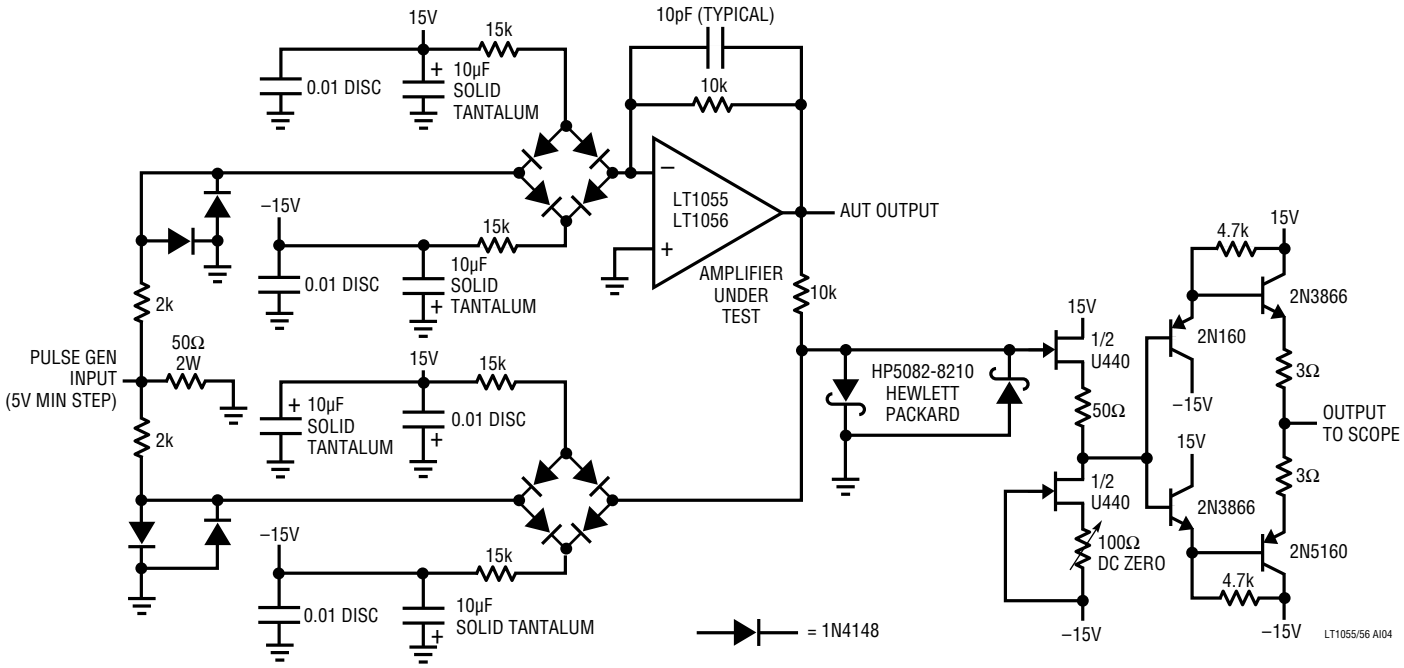
Settling time is measured in the test circuit shown. This test configuration has two features which eliminate problems common to settling time measurments: (1) probe capacitance is isolated from the "false summing" node, and (2) it does not require a "flat top" input pulse since the input pulse is merely used to steer current through the diode bridges. For more details, please see Application Note 10.

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx$ 4pF). In low closed-loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With R_S (C_S + C_{IN}) = R_FC_F, the effect of the feedback pole is completely removed.



Settling Time Test Circuit

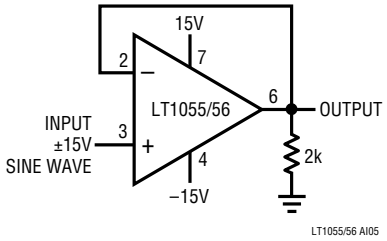


APPLICATIONS INFORMATION

Phase Reversal Protection

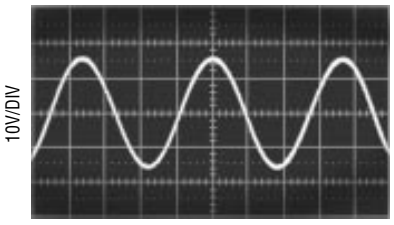
Most industry standard JFET input op amps (e.g., LF155/LF156, LF351, LF411, OP15/16) exhibit phase reversal at the output when the negitive common-mode limit at the input is exceeded (i.e., from –12V to –15V with ±15V supplies). This can cause lock-up in servo systems. As shown below, the LT1055/LT1056 does not have this problem due to unique phase reversal protection circuitry (Q1 on simplified schematic).

Voltage Follower with Input Exceeding the Negative Common-Mode Range



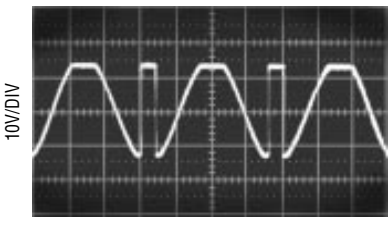
LT1055/56 AI05

Input



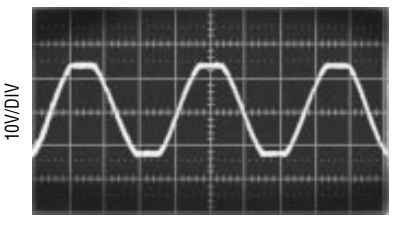
LT1055/56 AI06

Output (LF155/LF56, LF441, OP-15/OP-16)



LT1055/56 AI07

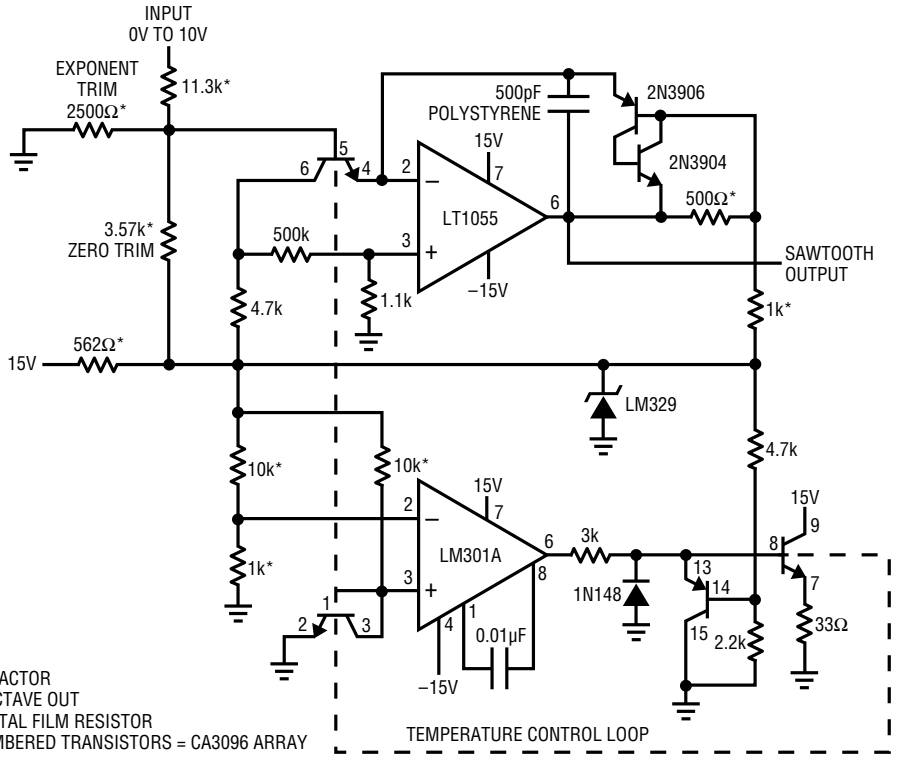
Output LT1055/LT1056



LT1055/56 AI08

TYPICAL APPLICATIONS †

Exponential Voltage-to-Frequency Converter for Music Synthesizers

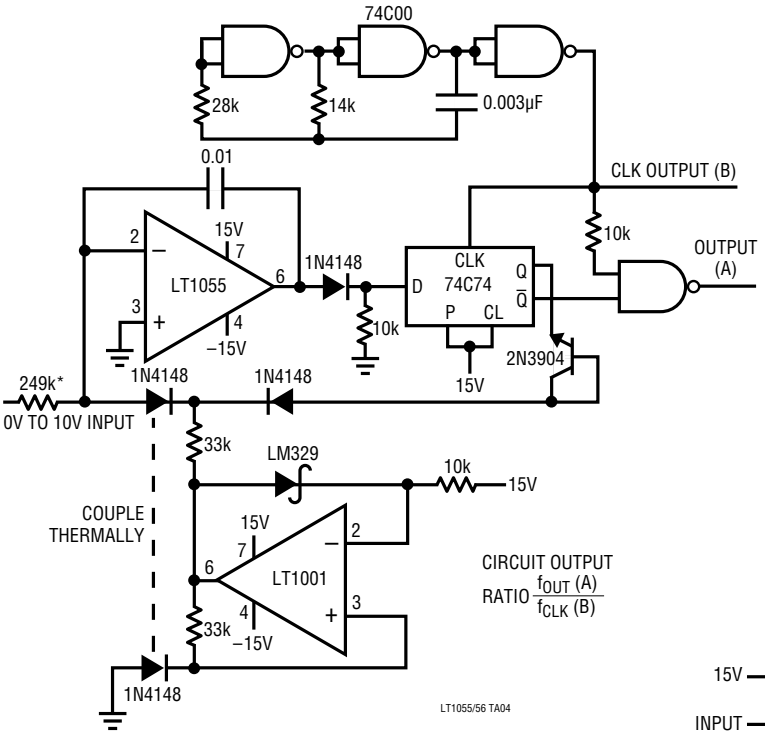


LT1055/56 TA03

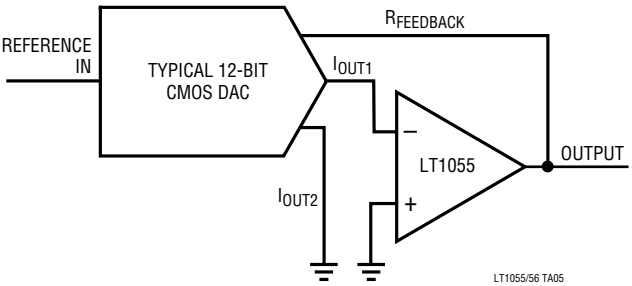
†For ten additional applications utilizing the LT1055 and LT1056, please see the LTC1043 data sheet and Application Note 3.

TYPICAL APPLICATIONS

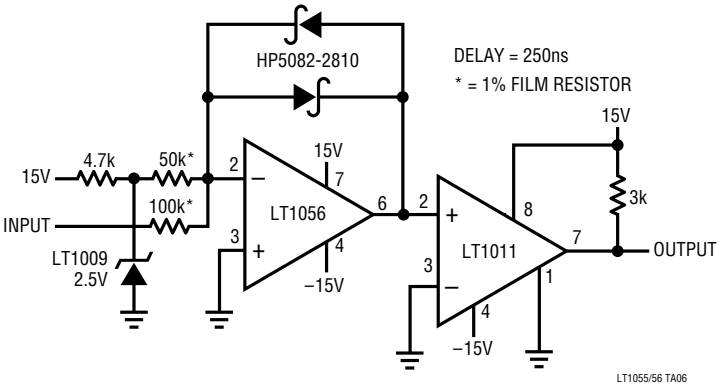
12-Bit Charge Balance A/D Converter



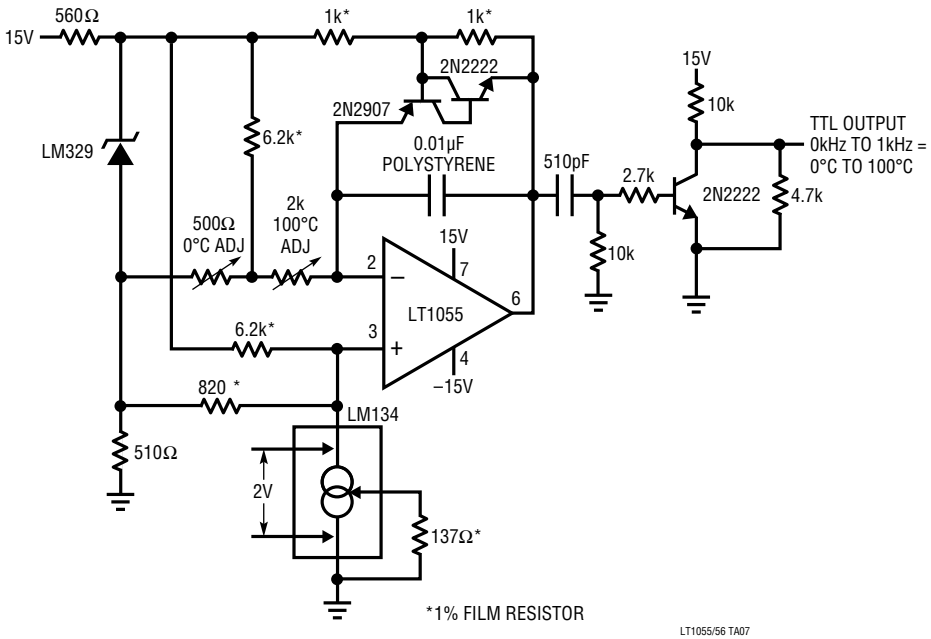
Fast "No Trims" 12-Bit Multiplying CMOS DAC Amplifier



Fast, 16-Bit Current Comparator

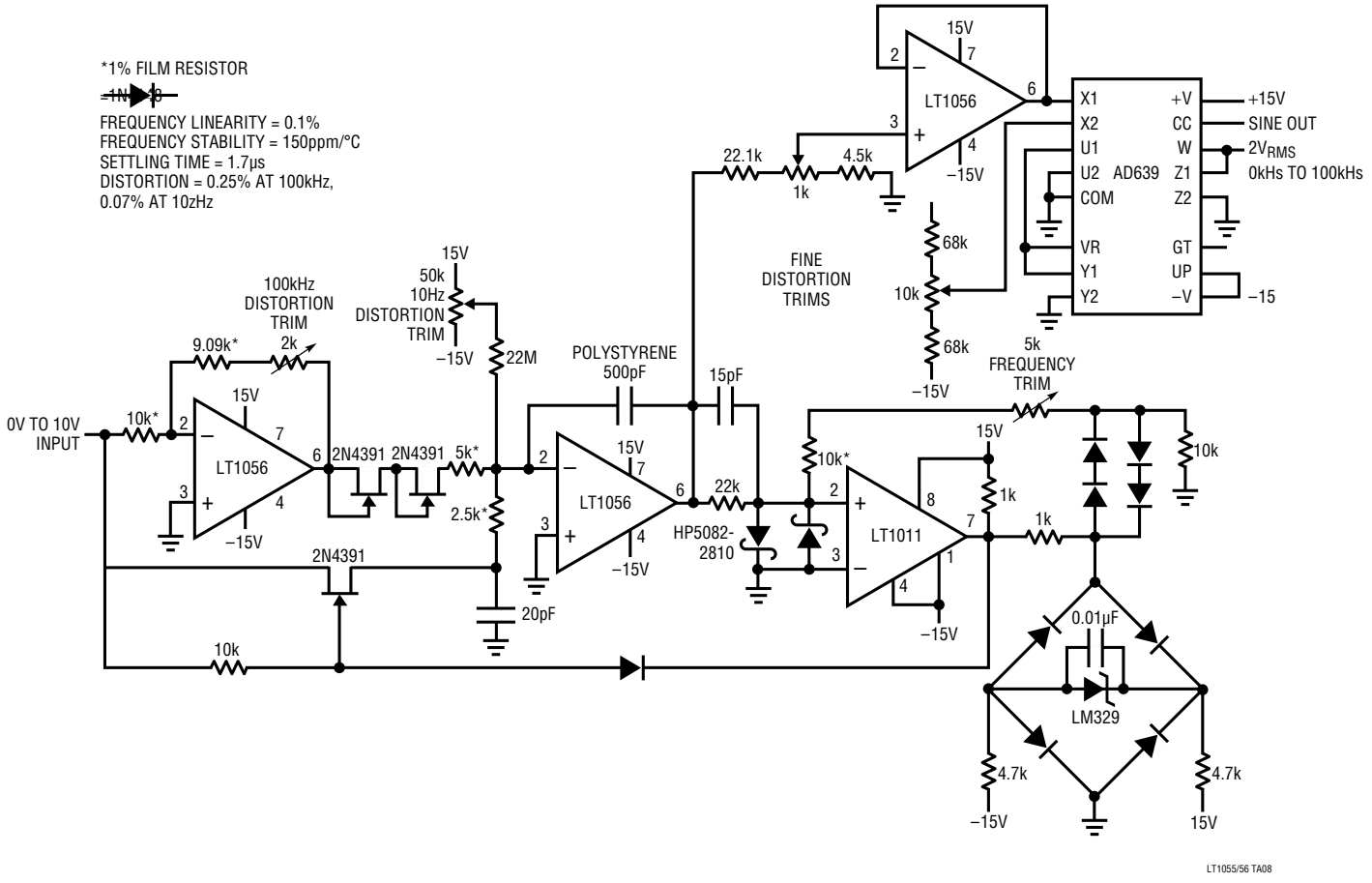


Temperature-to-Frequency Converter



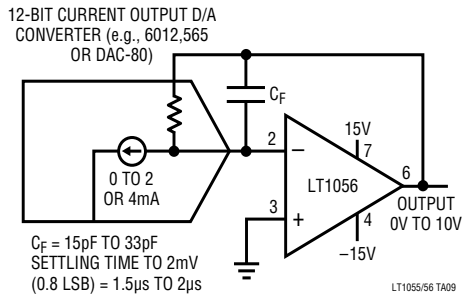
TYPICAL APPLICATIONS

100kHz Voltage Controlled Oscillator



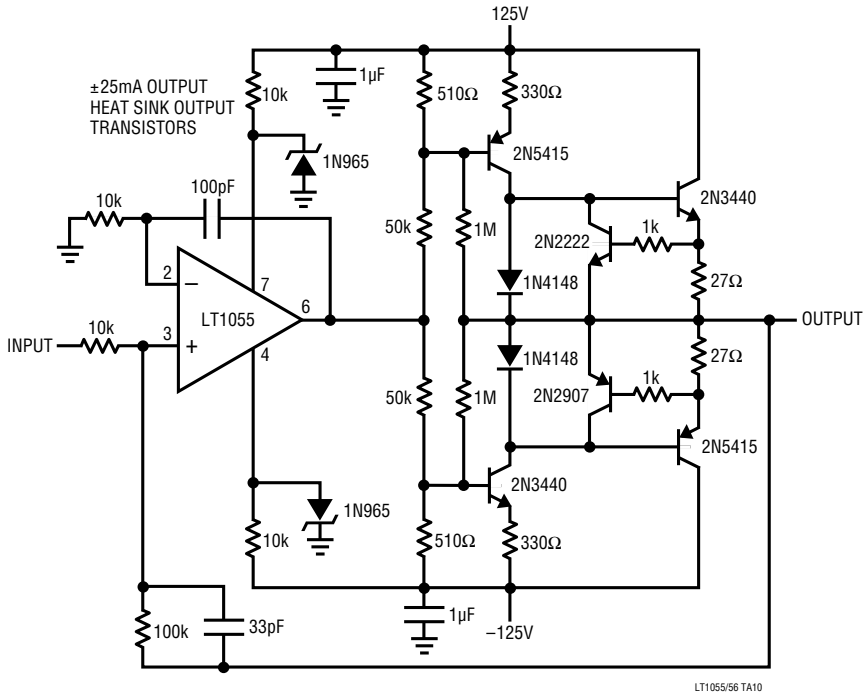
LT1055/56 TA08

12-Bit Voltage Output D/A Converter



LT1055/56 TA09

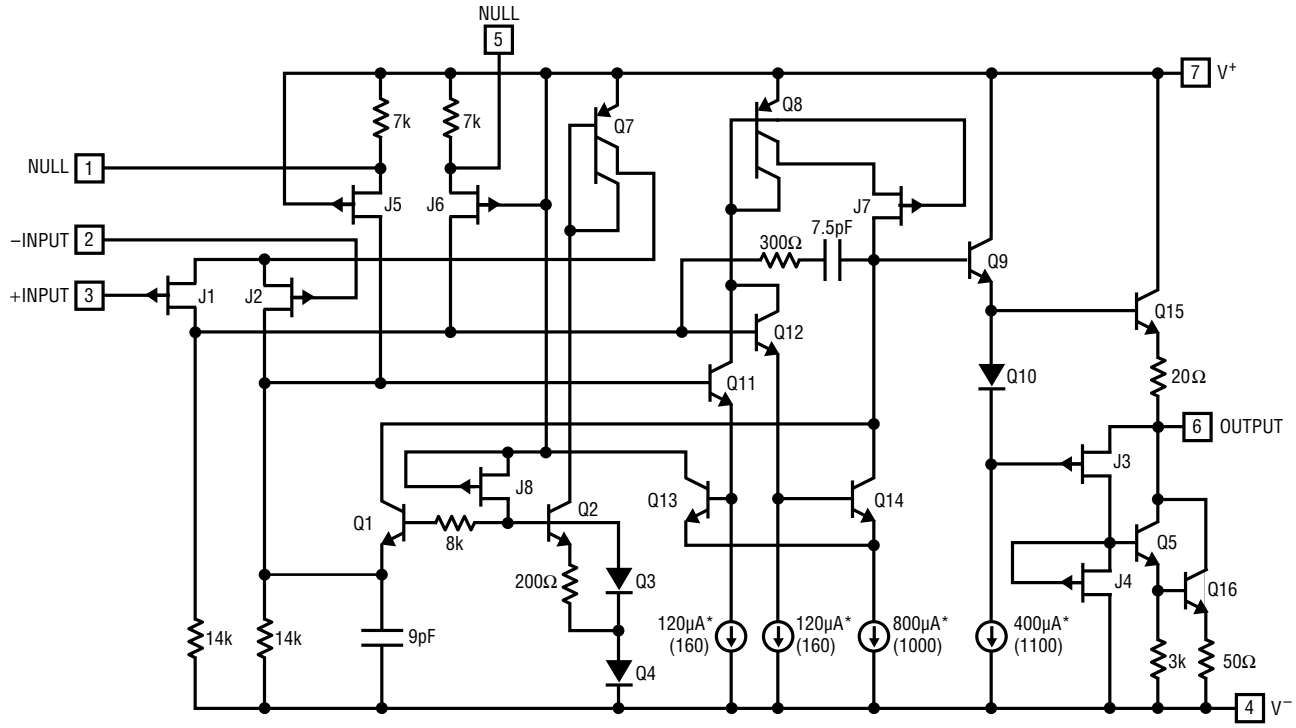
±120V Output Precision Op Amp



LT1055/56 TA10

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

SIMPLIFIED SCHEMATIC



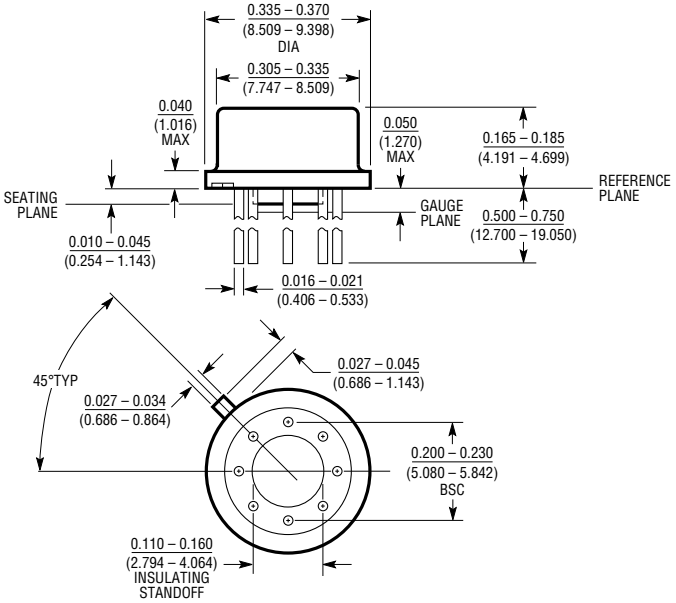
*CURRENTS AS SHOWN FOR LT1055. (X) = CURRENTS FOR LT1056.

LT1055/56 SCHM

PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

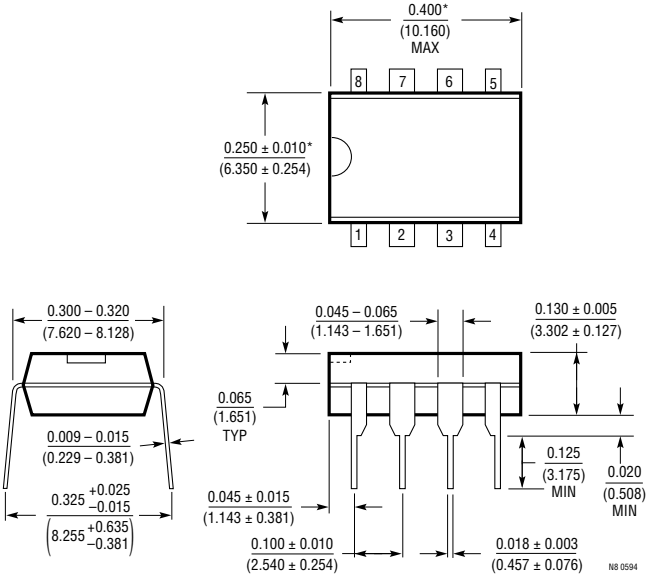
H Package Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN
THE REFERENCE PLANE AND SEATING PLANE.

H8(5) 0592

N8 Package
8-Lead Plastic



N8 0594

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

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