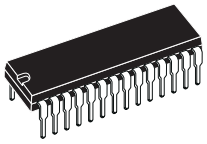
TDA7339

3 BAND DIGITAL CONTROLLED AUDIO PROCESSOR

PRODUCT PREVIEW

- THREE STEREO INPUT
- ONE RECORD OUTPUT
- ONE STEREO OUTPUT
- TWO INDEPENDENT VOLUME CONTROL IN 1.0dB STEPS
- TREBLE, MIDDLE AND BASS CONTROL IN 1.0dB STEPS
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I^2 CBUS



DIP28

ORDERING NUMBER: TDA7339

DESCRIPTION

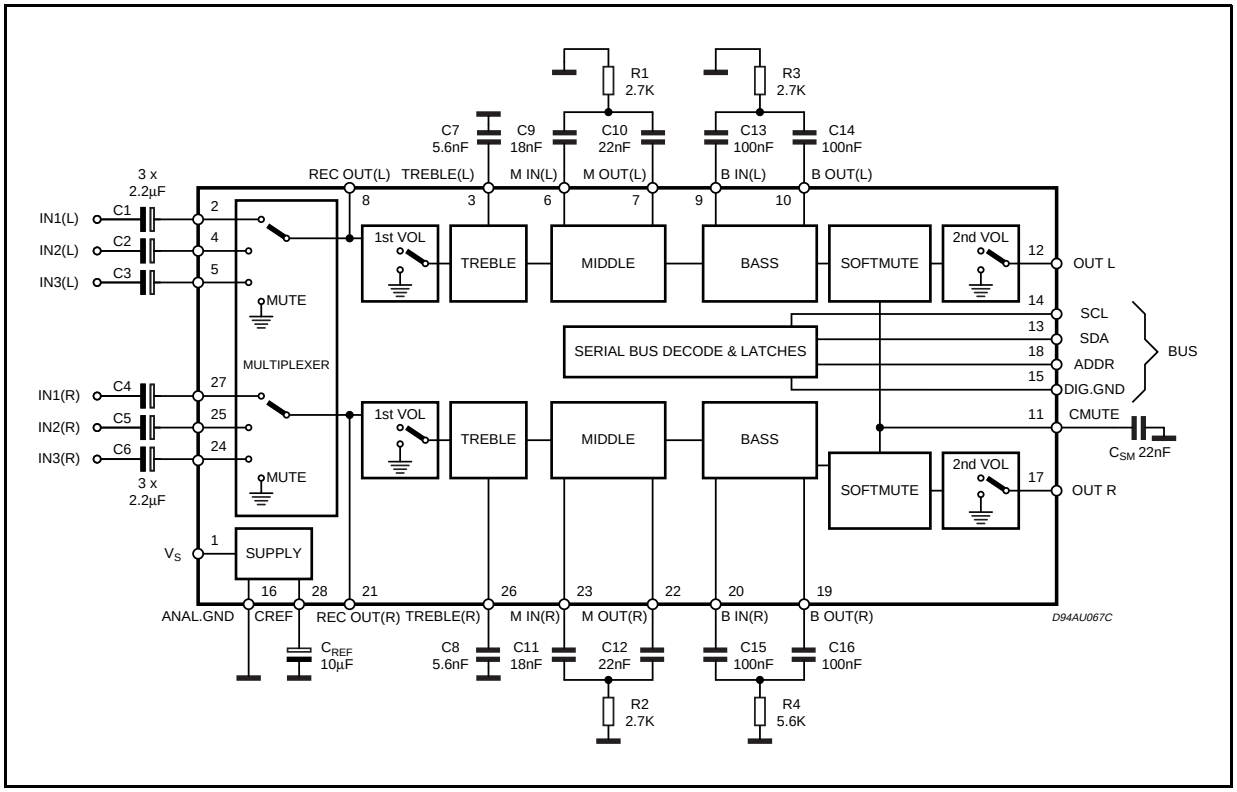
The TDA7339 is a volume and tone (bass , middle and treble) processor for quality audio application in car radio and Hi-Fi system.

Control is accomplished by serial I^2C bus microprocessor interface.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/MOS Technology, Low Distortion, Low Noise and Low DC stepping are obtained.

BLOCK DIAGRAM

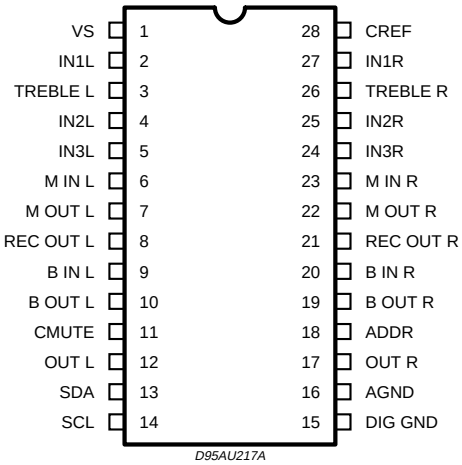


This is preliminary information on a new product now in development. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-pins	65	°C/W

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01	0.08	%
S/N	Signal to Noise Ratio		106		dB
S_C	Channel Separation f = 1KHz		100		dB
	1st and 2nd Volume Control 1dB step	-47		0	dB
	Bass, Middle and Treble Control 1dB step	-14		+14	dB
	Mute Attenuation		100		dB

ELECTRICAL CHARACTERISTICS (V_S = 9V; R_L = 10KΩ; f = 1KHz; all control = flat (G = 0); T_{amb} = 25°C Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUTS						
R_{in}	Input Resistance		35	50	65	KΩ
1st VOLUME CONTROL						
C_{RANGE}	Control Range		45	47	49	dB
A_{VMAX}	Maximum Attenuation		45	47	49	dB
A_{step}	Step Resolution		0.5	1.0	1.5	dB
E_A	Attenuation Set Error	G = 0 to -24dB	-1.0		1.0	dB
		G = -24 to -47dB	-1.5		1.5	dB
E_t	Tracking Error	G = 0 to -24dB			1	dB
		G = 24 to -47dB			2	dB
A_{mute}	Mute Attenuation		80	100		dB
V_{DC}	DC Steps	Adiacent Attenuation Steps		0	3	mV
		From 0dB to A_{VMAX}		0.5	5	mV
2nd VOLUME CONTROL						
C_{RANGE}	Control Range		45	47	49	dB
A_{VMAX}	Maximum Attenuation		45	47	49	dB
A_{step}	Step Resolution		0.5	1.0	1.5	dB
E_A	Attenuation Set Error	G = 0 to -24dB	-1.0		1.0	dB
		G = -24 to -47dB	-1.5		1.5	dB
E_t	Tracking Error	G = 0 to -24dB			1	dB
		G = 24 to -47dB			2	dB
A_{MUTE}	Mute Attenuation		80	100		dB
V_{DC}	DC Steps	Adiacent Attenuation Steps		0	3	mV
		From 0dB to A_{VMAX}		0.5	5	mV
BASS						
R_b	Internal Feedback Resistance		32	44	56	KΩ
C_{RANGE}	Control Range		±11.5	±14	±16	dB
A_{step}	Step Resolution		0.5	1	1.5	dB
MIDDLE						
R_b	Internal Feedback Resistance		18	25	32	KΩ
C_{RANGE}	Control Range		±11.5	±14	±16	dB
A_{step}	Step Resolution		0.5	1	1.5	dB
TREBLE						
C_{RANGE}	Control Range		±13	±14	±15	dB
A_{step}	Step Resolution		0.5	1	1.5	dB
SUPPLY						
V_S	Supply Voltage (note1)		6	9	10.5	V
I_S	Supply Current		4	7	10	mA
SVR	Ripple Rejection		60	90		dB
SOFT MUTE						
A_{MUTE}	Mute Attenuation		45	60		dB
t_D	Delay Time	C_{SM} = 22µF; 0 to 20dB; I = I_{MAX}	0.8	1.5	2	ms
		C_{SM} = 22µF; 0 to 20dB; I = I_{MIN}	15	25	45	ms

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AUDIO OUTPUT						
V_{clip}	Clipping Level	d = 0.3%	2	2.6		Vrms
R_{Ol}	Output Load Resistance		2			KΩ
R_O	Output Impedance		100	180	300	Ω
V_{DC}	DC Voltage Level			3.8		V
GENERAL						
e_{NO}	Output Noise	All Gains 0dB (B = 20 to 20kHz flat)		5	15	µV
E_t	Total Tracking Error	A_V = 0 to -24dB		0	1	dB
		A_V = -24 to -47dB		0	2	dB
S/N	Signal to Noise Ratio	All Gains = 0dB; $V_O = 1V_{rms}$		106		dB
S_C	Channel Separation		80	100		dB
d	Distortion	A_V = 0; $V_{in} = 1V_{rms}$		0.01	0.08	%
BUS INPUTS						
V_{il}	Input Low Voltage				1	V
V_{ih}	Input High Voltage		3			V
I_{in}	Input Current	V_{in} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA		0.4	0.8	V

NOTE 1: the device is functionally good at Vs = 5V. A step down, on V_S, to 4V does't reset the device.

I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7319 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

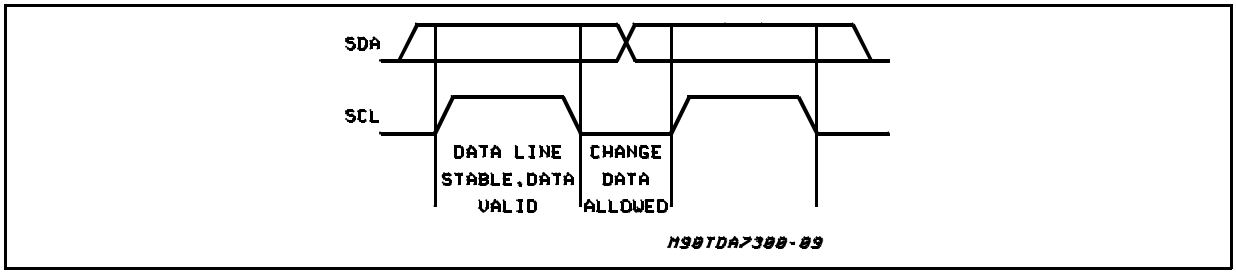
The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

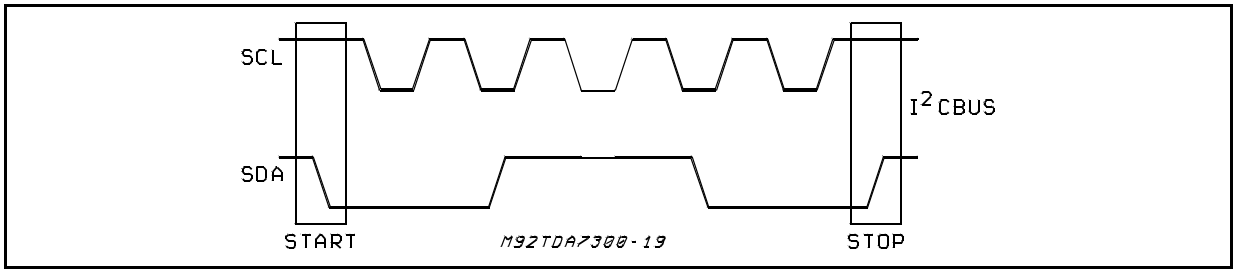
Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it generates the 9th clock pulse without checking the slave acknowledging, and then sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

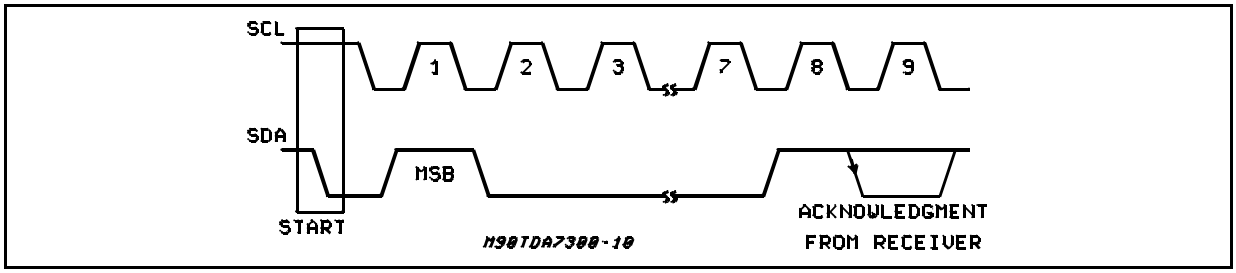
Data Validity on the I²CBUS



Timing Diagram of I²CBUS



Acknowledge on the I²CBUS

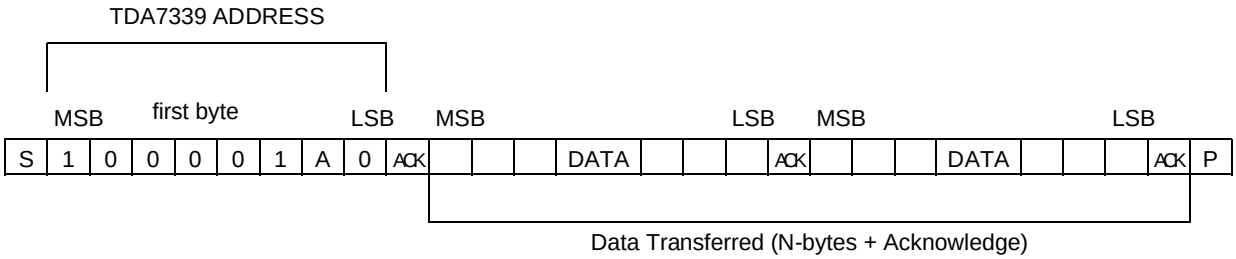


SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7339 address (the 8th bit of the byte must be 0). The TDA7339 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address

1 MSB	0	0	0	0	1	A	0 LSB

A = Logic level ON pin ADDR

FUNCTION CODES

	MSB	F6	F5	F4	F3	F2	F1	LSB
1st VOLUME	0	F6	F5	F4	F3	F2	F1	0
2nd VOLUME	0	F6	F5	F4	F3	F2	F1	1
TREBLE	1	0	0	F4	F3	F2	F1	F0
MIDDLE	1	0	1	F4	F3	F2	F1	F0
BASS	1	1	0	F4	F3	F2	F1	F0
MUTMUX	1	1	1	F4	F3	F2	F1	F0

POWER ON RESET:
1st volume = 2nd volume = Mute
Treble = Middle = Bass = -14dB
Mutmux = Active Input IN 1

1st VOLUME CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
0							0	step 1dB
				0	0	0		0dB
				0	0	1		-1dB
				0	1	0		-2dB
				0	1	1		-3dB
				1	0	0		-4dB
				1	0	1		-5dB
				1	1	0		-6dB
				1	1	1		-7dB
0							0	step 8dB
	0	0	0					0dB
	0	0	1					-8dB
	0	1	0					-16dB
	0	1	1					-24dB
	1	0	0					-32dB
	1	0	1					-40dB
	1	1	1					MUTE

2nd VOLUME CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
0							1	step 1dB
				0	0	0		0dB
				0	0	1		-1dB
				0	1	0		-2dB
				0	1	1		-3dB
				1	0	0		-4dB
				1	0	1		-5dB
				1	1	0		-6dB
				1	1	1		-7dB
0							1	step 8dB
	0	0	0					0dB
	0	0	1					-8dB
	0	1	0					-16dB
	0	1	1					-24dB
	1	0	0					-32dB
	1	0	1					-40dB
	1	1	1					MUTE

TREBLE CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	0	0						TREBLE BOOST
			0	0	0	0	0	0dB
			0	0	0	0	1	1dB
			0	0	0	1	0	2dB
			0	0	0	1	1	3dB
			0	0	1	0	0	4dB
			0	0	1	0	1	5dB
			0	0	1	1	0	6dB
			0	0	1	1	1	7dB
			0	1	0	0	0	8dB
			0	1	0	0	1	9dB
			0	1	0	1	0	10dB
			0	1	0	1	1	11dB
			0	1	1	0	0	12dB
			0	1	1	0	1	13dB
			0	1	1	1	0	14dB
			0	1	1	1	1	14dB
1	0	0						TREBLE CUT
			1	0	0	0	0	0dB
			1	0	0	0	1	-1dB
			1	0	0	1	0	-2dB
			1	0	0	1	1	-3dB
			1	0	1	0	0	-4dB
			1	0	1	0	1	-5dB
			1	0	1	1	0	-6dB
			1	0	1	1	1	-7dB
			1	1	0	0	0	-8dB
			1	1	0	0	1	-9dB
			1	1	0	1	0	-10dB
			1	1	0	1	1	-11dB
			1	1	1	0	0	-12dB
			1	1	1	0	1	-13dB
			1	1	1	1	0	-14dB
			1	1	1	1	1	-14dB

MIDDLE CODES

MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	0	1						MIDDLE BOOST
			0	0	0	0	0	0dB
			0	0	0	0	1	1dB
			0	0	0	1	0	2dB
			0	0	0	1	1	3dB
			0	0	1	0	0	4dB
			0	0	1	0	1	5dB
			0	0	1	1	0	6dB
			0	0	1	1	1	7dB
			0	1	0	0	0	8dB
			0	1	0	0	1	9dB
			0	1	0	1	0	10dB
			0	1	0	1	1	11dB
			0	1	1	0	0	12dB
			0	1	1	0	1	13dB
			0	1	1	1	0	14dB
			0	1	1	1	1	14dB
1	0	1						MIDDLE CUT
			1	0	0	0	0	0dB
			1	0	0	0	1	-1dB
			1	0	0	1	0	-2dB
			1	0	0	1	1	-3dB
			1	0	1	0	0	-4dB
			1	0	1	0	1	-5dB
			1	0	1	1	0	-6dB
			1	0	1	1	1	-7dB
			1	1	0	0	0	-8dB
			1	1	0	0	1	-9dB
			1	1	0	1	0	-10dB
			1	1	0	1	1	-11dB
			1	1	1	0	0	-12dB
			1	1	1	0	1	-13dB
			1	1	1	1	0	-14dB
			1	1	1	1	1	-14dB

BASS CODES

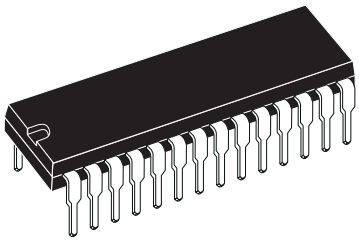
MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	1	0						BASS BOOST
			0	0	0	0	0	0dB
			0	0	0	0	1	1dB
			0	0	0	1	0	2dB
			0	0	0	1	1	3dB
			0	0	1	0	0	4dB
			0	0	1	0	1	5dB
			0	0	1	1	0	6dB
			0	0	1	1	1	7dB
			0	1	0	0	0	8dB
			0	1	0	0	1	9dB
			0	1	0	1	0	10dB
			0	1	0	1	1	11dB
			0	1	1	0	0	12dB
			0	1	1	0	1	13dB
			0	1	1	1	0	14dB
			0	1	1	1	1	14dB
1	1	0						BASS CUT
			1	0	0	0	0	0dB
			1	0	0	0	1	-1dB
			1	0	0	1	0	-2dB
			1	0	0	1	1	-3dB
			1	0	1	0	0	-4dB
			1	0	1	0	1	-5dB
			1	0	1	1	0	-6dB
			1	0	1	1	1	-7dB
			1	1	0	0	0	-8dB
			1	1	0	0	1	-9dB
			1	1	0	1	0	-10dB
			1	1	0	1	1	-11dB
			1	1	1	0	0	-12dB
			1	1	1	0	1	-13dB
			1	1	1	1	0	-14dB
			1	1	1	1	1	-14dB

MUTMUX CODES

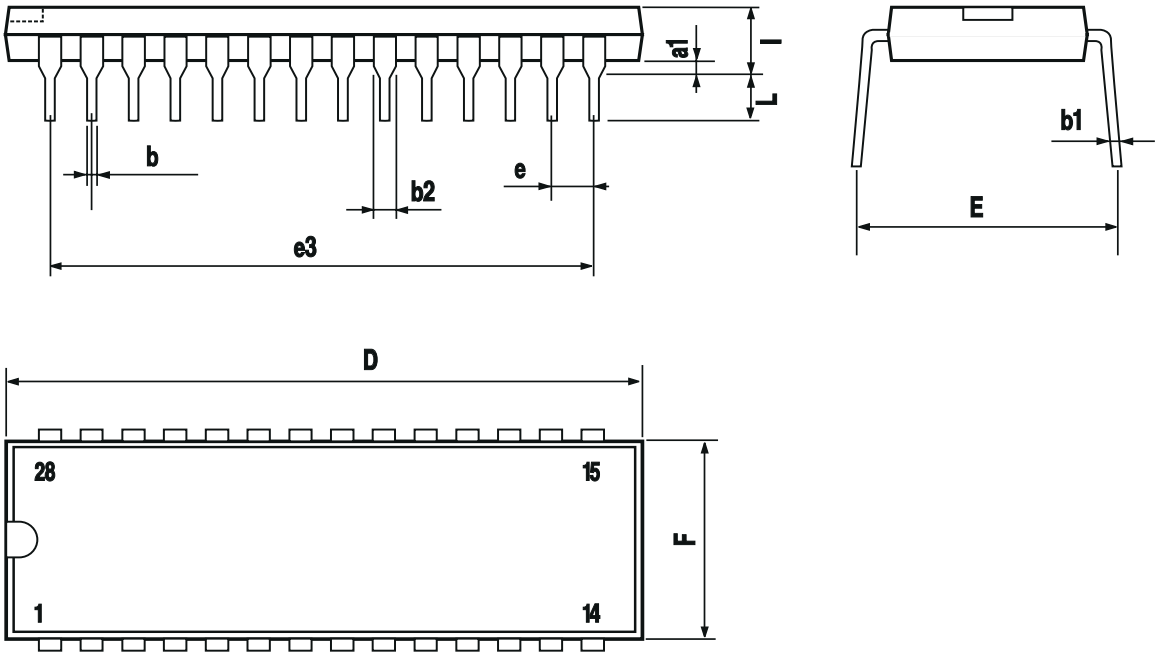
MSB	F6	F5	F4	F3	F2	F1	LSB	FUNCTION
1	1	1						INPUTS
			X	X	X	0	0	SLOW SOFT MUTE SLOPE ($I=I_{MIN}$)
			X	X	X	0	1	FAST SOFT MUTE SLOPE ($I=I_{MAN}$)
			X	X	X	1	X	SOFT MUTE OFF
			X	0	0			NOT ALLOWED
			X	0	1			IN3
			X	1	0			IN2
			X	1	1			IN1

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

OUTLINE AND MECHANICAL DATA



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