TOP221-227

TOPSwitch®-II Family

Three-terminal Off-line PWM Switch

Product Highlights

- Lowest cost, lowest component count switcher solution
- Cost competitive with linears above 5W
- Very low AC/DC losses – up to 90% efficiency
- Built-in Auto-restart and Current limiting
- Latching Thermal shutdown for system level protection
- Implements Flyback, Forward, Boost or Buck topology
- Works with primary or opto feedback
- Stable in discontinuous or continuous conduction mode
- Source connected tab for low EMI
- Circuit simplicity and Design Tools reduce time to market

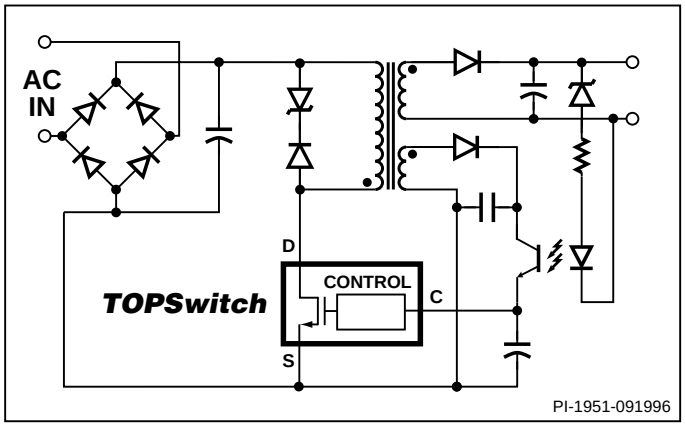


Figure 1. Typical Flyback Application.

Description

The second generation *TOPSwitch-II* family is more cost effective and provides several enhancements over the first generation *TOPSwitch* family. The *TOPSwitch-II* family extends the power range from 100W to 150W for 100/115/230 VAC input and from 50W to 90W for 85-265 VAC universal input. This brings *TOPSwitch* technology advantages to many new applications, i.e. TV, Monitor, Audio amplifiers, etc. Many significant circuit enhancements that reduce the sensitivity to board layout and line transients now make the design even easier. The standard 8L PDIP package option reduces cost in lower power, high efficiency applications. The internal lead frame of this package uses six of its pins to transfer heat from the chip directly to the board, eliminating the cost of a heat sink. *TOPSwitch* incorporates all functions necessary for a switched mode control system into a three terminal monolithic IC: power MOSFET, PWM controller, high voltage start up circuit, loop compensation and fault protection circuitry.

OUTPUT POWER TABLE

TO-220 (Y) Package[1]			8L PDIP (P) or 8L SMD (G) Package[2]		
PART ORDER NUMBER	Single Voltage Input[3] 100/115/230 VAC ±15% P_{MAX}[4,6]	Wide Range Input 85 to 265 VAC P_{MAX}[4,6]	PART ORDER NUMBER	Single Voltage Input[3] 100/115/230 VAC ±15% P_{MAX}[5,6]	Wide Range Input 85 to 265 VAC P_{MAX}[5,6]
TOP221Y	12 W	7 W	TOP221P or TOP221G	9 W	6 W
TOP222Y	25 W	15 W	TOP222P or TOP222G	15 W	10 W
TOP223Y	50 W	30 W	TOP223P or TOP223G	25 W	15 W
TOP224Y	75 W	45 W	TOP224P or TOP224G	30 W	20 W
TOP225Y	100 W	60 W			
TOP226Y	125 W	75 W			
TOP227Y	150 W	90 W			

Notes: **1**. Package outline: TO-220/3 **2**. Package Outline: DIP-8 or SMD-8 **3.** 100/115 VAC with doubler input **4**. Assumes appropriate heat sinking to keep the maximum *TOPSwitch* junction temperature below 100 °C. **5**. Soldered to 1 sq. in.(6.45 cm^2), 2 oz. copper clad (610 gm/m^2) **6**. P_{MAX} is the maximum practical continuous power output level for conditions shown. The continuous power capability in a given application depends on thermal environment, transformer design, efficiency required, minimum specified input voltage, input storage capacitance, etc. **7**. Refer to key application considerations section when using *TOPSwitch-II* in an existing *TOPSwitch* design.

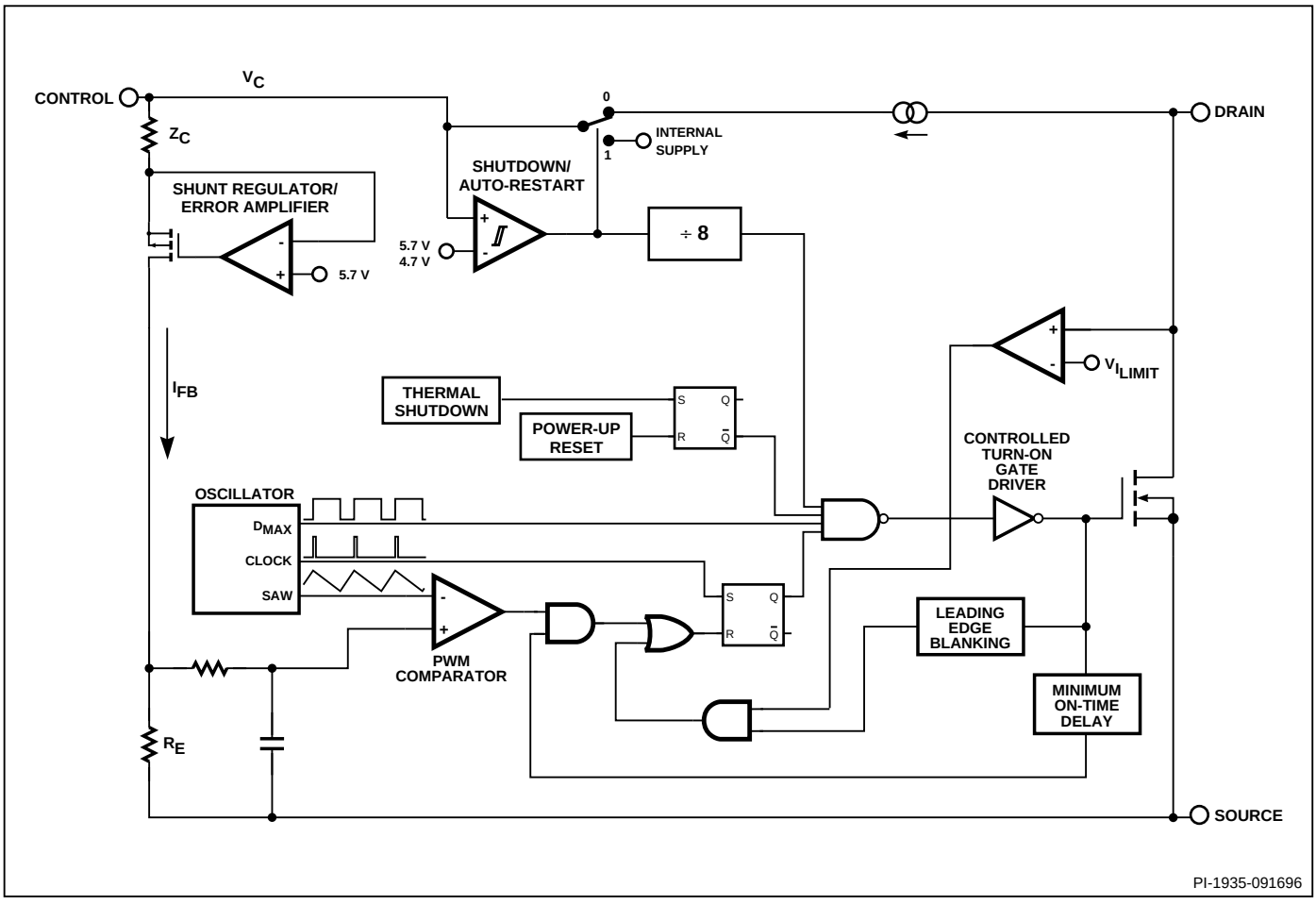


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN Pin:
Output MOSFET drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.

CONTROL Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also used as the connection point for the supply bypass and auto-restart/ compensation capacitor.

SOURCE Pin:
Y package – Output MOSFET source connection for high voltage power return. Primary side circuit common and reference point.

P and G package – Primary side control circuit common and reference point.

SOURCE (HV RTN) Pin: (P and G package only)
Output MOSFET source connection for high voltage power return.

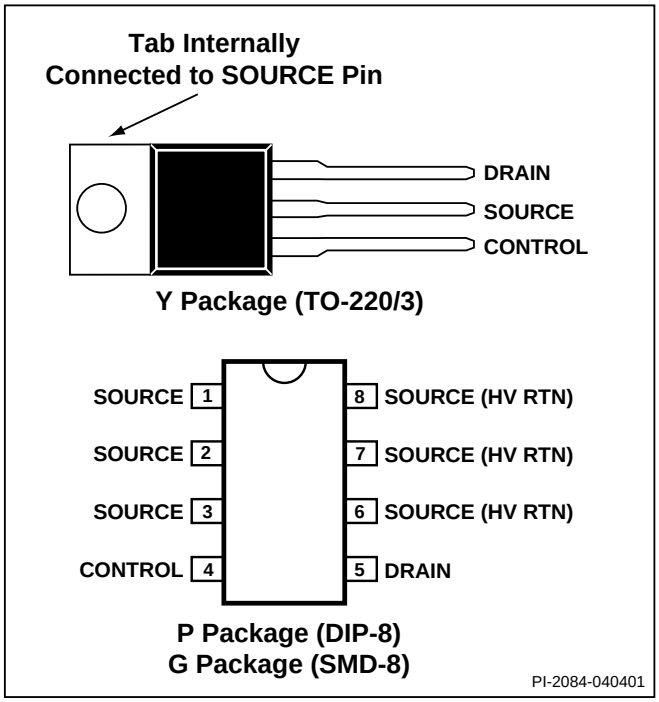


Figure 3. Pin Configuration.

TOPSwitch-II Family Functional Description

TOPSwitch is a self biased and protected linear control current-to-duty cycle converter with an open drain output. High efficiency is achieved through the use of CMOS and integration of the maximum number of functions possible. CMOS process significantly reduces bias currents as compared to bipolar or discrete solutions. Integration eliminates external power resistors used for current sensing and/or supplying initial start-up bias current.

During normal operation, the duty cycle of the internal output MOSFET decreases linearly with increasing CONTROL pin current as shown in Figure 4. To implement all the required control, bias, and protection functions, the DRAIN and CONTROL pins each perform several functions as described below. Refer to Figure 2 for a block diagram and to Figure 6 for timing and voltage waveforms of the *TOPSwitch* integrated circuit.

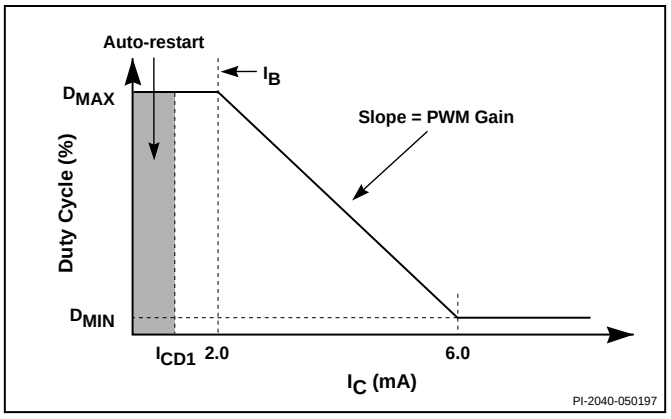


Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.

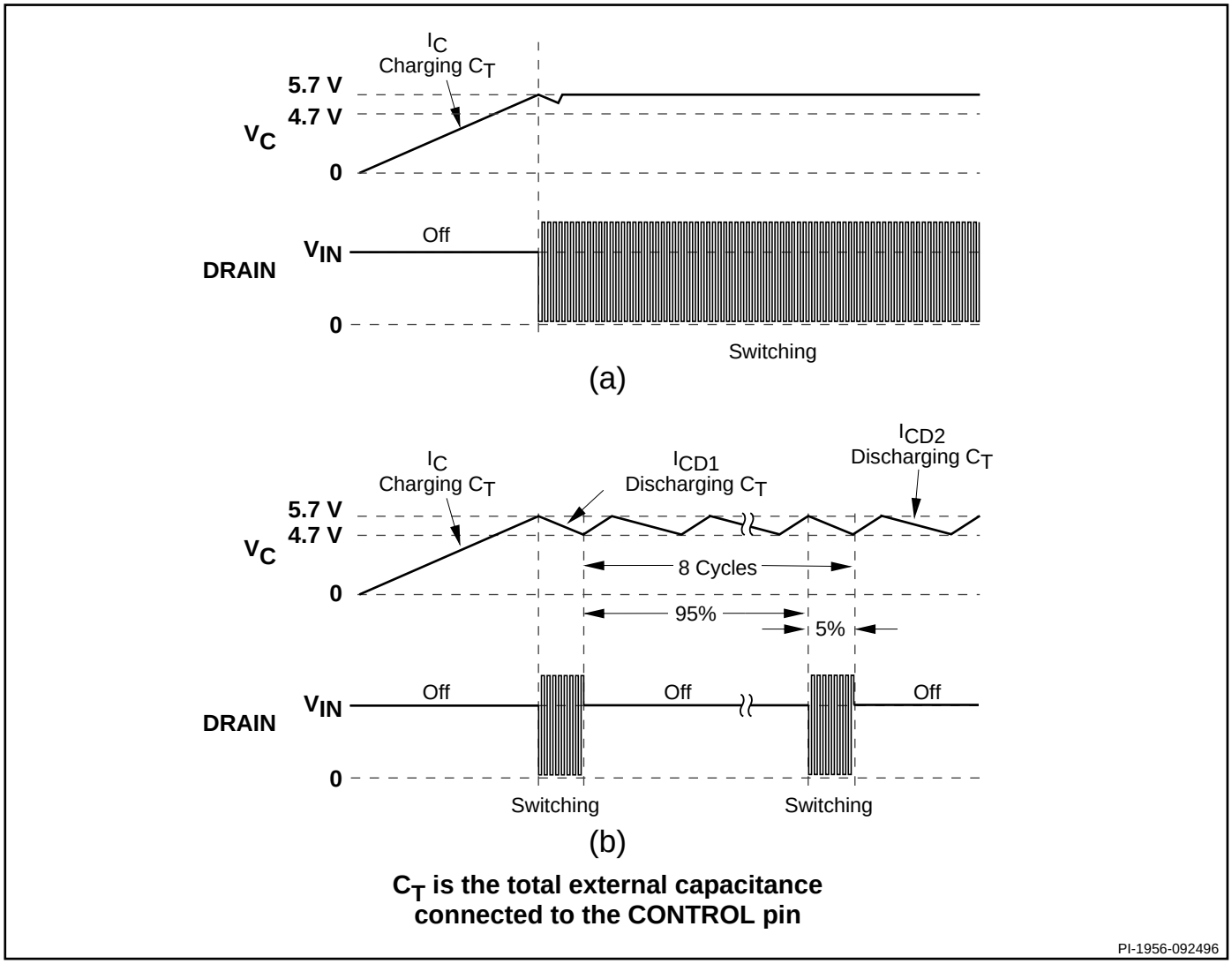


Figure 5. Start-up Waveforms for (a) Normal Operation and (b) Auto-restart.

TOPSwitch-II Family Functional Description (cont.)

Control Voltage Supply

CONTROL pin voltage V_C is the supply or bias voltage for the controller and driver circuitry. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the gate drive current. The total amount of capacitance connected to this pin (C_T) also sets the auto-restart timing as well as control loop compensation. V_C is regulated in either of two modes of operation. Hysteretic regulation is used for initial start-up and overload operation. Shunt regulation is used to separate the duty cycle error signal from the control circuit supply current. During start-up, CONTROL pin current is supplied from a high-voltage switched current source connected internally between the DRAIN and CONTROL pins. The current source provides sufficient current to supply the control circuitry as well as charge the total external capacitance (C_T).

The first time V_C reaches the upper threshold, the high-voltage current source is turned off and the PWM modulator and output transistor are activated, as shown in Figure 5(a). During normal operation (when the output voltage is regulated) feedback control current supplies the V_C supply current. The shunt regulator keeps V_C at typically 5.7 V by shunting CONTROL pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor R_E. The low dynamic impedance of this pin (Z_C) sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance of the CONTROL pin together with the external resistance and capacitance determines the control loop compensation of the power system.

If the CONTROL pin total external capacitance (C_T) should discharge to the lower threshold, the output MOSFET is turned off and the control circuit is placed in a low-current standby mode. The high-voltage current source turns on and charges the external capacitance again. Charging current is shown with a negative polarity and discharging current is shown with a positive polarity in Figure 6. The hysteretic auto-restart comparator keeps V_C within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off as shown in Figure 5(b). The auto-restart circuit has a divide-by-8 counter which prevents the output MOSFET from turning on again until eight discharge-charge cycles have elapsed. The counter effectively limits *TOPSwitch* power dissipation by reducing the auto-restart duty cycle to typically 5%. Auto-restart continues to cycle until output voltage regulation is again achieved.

Bandgap Reference

All critical *TOPSwitch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current source which is trimmed to accurately set the oscillator frequency and MOSFET gate drive current.

Oscillator

The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency of 100 kHz was chosen to minimize EMI and maximize efficiency in power supply applications. Trimming of the current reference improves the frequency accuracy.

Pulse Width Modulator

The pulse width modulator implements a voltage-mode control loop by driving the output MOSFET with a duty cycle inversely proportional to the current into the CONTROL pin which generates a voltage error signal across R_E. The error signal across R_E is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. The maximum duty cycle is set by the symmetry of the internal oscillator. The modulator has a minimum ON-time to keep the current consumption of the *TOPSwitch* independent of the error signal. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

Gate Driver

The gate driver is designed to turn the output MOSFET on at a controlled rate to minimize common-mode EMI. The gate drive current is trimmed for improved accuracy.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary feedback applications. The shunt regulator voltage is accurately derived from the temperature compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through R_E as a voltage error signal.

Cycle-By-Cycle Current Limit

The cycle by cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain-source voltage, $V_{DS(ON)}$ with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature

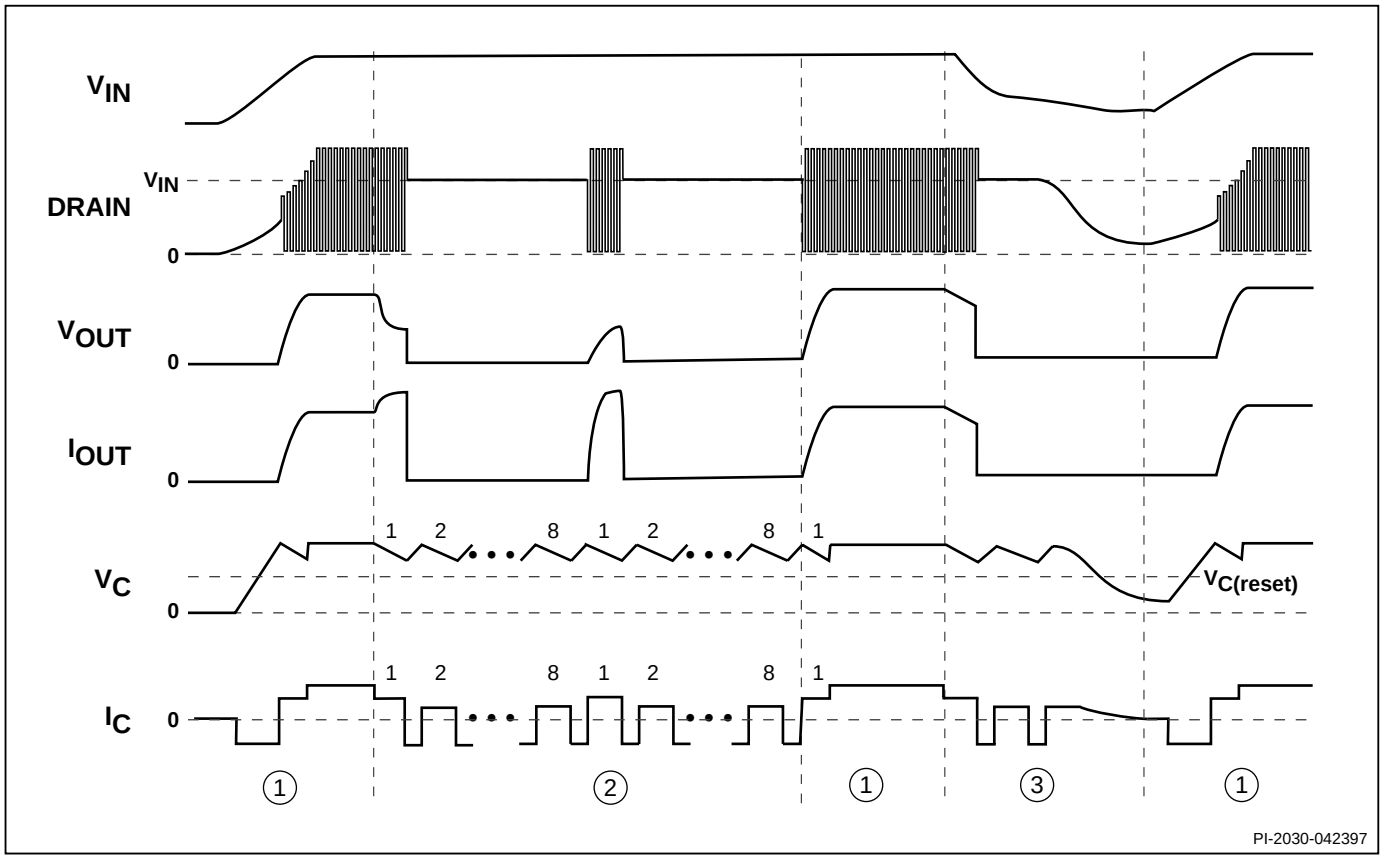


Figure 6. Typical Waveforms for (1) Normal Operation, (2) Auto-restart, and (3) Power Down Reset.

compensated to minimize variation of the effective peak current limit due to temperature related changes in output MOSFET $R_{DS(ON)}$.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

The current limit can be lower for a short period after the leading edge blanking time as shown in Figure 12. This is due to dynamic characteristics of the MOSFET. To avoid triggering the current limit in normal operation, the drain current waveform should stay within the envelope shown.

Shutdown/Auto-restart

To minimize *TOPSwitch* power dissipation, the shutdown/auto-restart circuit turns the power supply on and off at an auto-restart duty cycle of typically 5% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode described above. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Overtemperature Protection

Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (typically 135 °C). Activating the power-up reset circuit by removing and restoring input power or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode and a 4.7 V to 5.7 V (typical) sawtooth waveform is present on the CONTROL pin when the power supply is latched off.

High-voltage Bias Current Source

This current source biases *TOPSwitch* from the DRAIN pin and charges the CONTROL pin external capacitance (C_T) during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart and overtemperature latched shutdown. The current source is switched on and off with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge (I_C) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching.

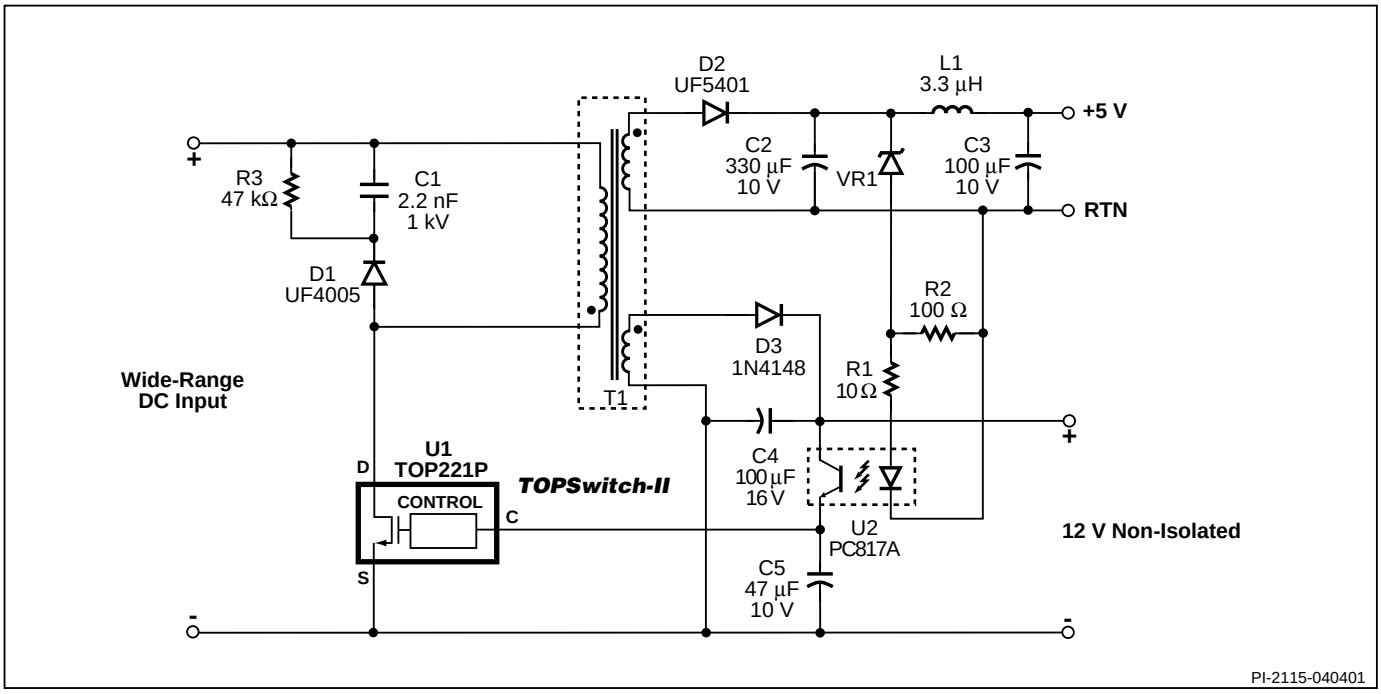


Figure 7. Schematic Diagram of a 4 W TOPSwitch-II Standby Power Supply using an 8 lead PDIP.

Application Examples

Following are just two of the many possible *TOPSwitch* implementations. Refer to the Data Book and Design Guide for additional examples.

4 W Standby Supply using 8 Lead PDIP

Figure 7 shows a 4 W standby supply. This supply is used in appliances where certain standby functions (e.g. real time clock, remote control port) must be kept active even while the main power supply is turned off.

The 5 V secondary is used to supply the standby function and the 12 V non-isolated output is used to supply power for the PWM controller of the main power supply and other primary side functions.

For this application the input rectifiers and input filter are sized for the main supply and are not shown. The input DC rail may vary from 100 V to 380 V DC which corresponds to the full universal AC input range. The TOP221 is packaged in an 8 pin power DIP package.

The output voltage (5 V) is directly sensed by the Zener diode (VR1) and the optocoupler (U2). The output voltage is determined by the sum of the Zener voltage and the voltage drop across the LED of the optocoupler (the voltage drop across R1 is negligible). The output transistor of the optocoupler drives the CONTROL pin of the TOP221. C5 bypasses the CONTROL pin and provides control loop compensation and sets the auto-restart frequency.

The transformer's leakage inductance voltage spikes are snubbed by R3 and C1 through diode D1. The bias winding is rectified and filtered by D3 and C4 providing a non-isolated 12 V output which is also used to bias the collector of the optocoupler's output transistor. The isolated 5 V output winding is rectified by D2 and filtered by C2, L1 and C3.

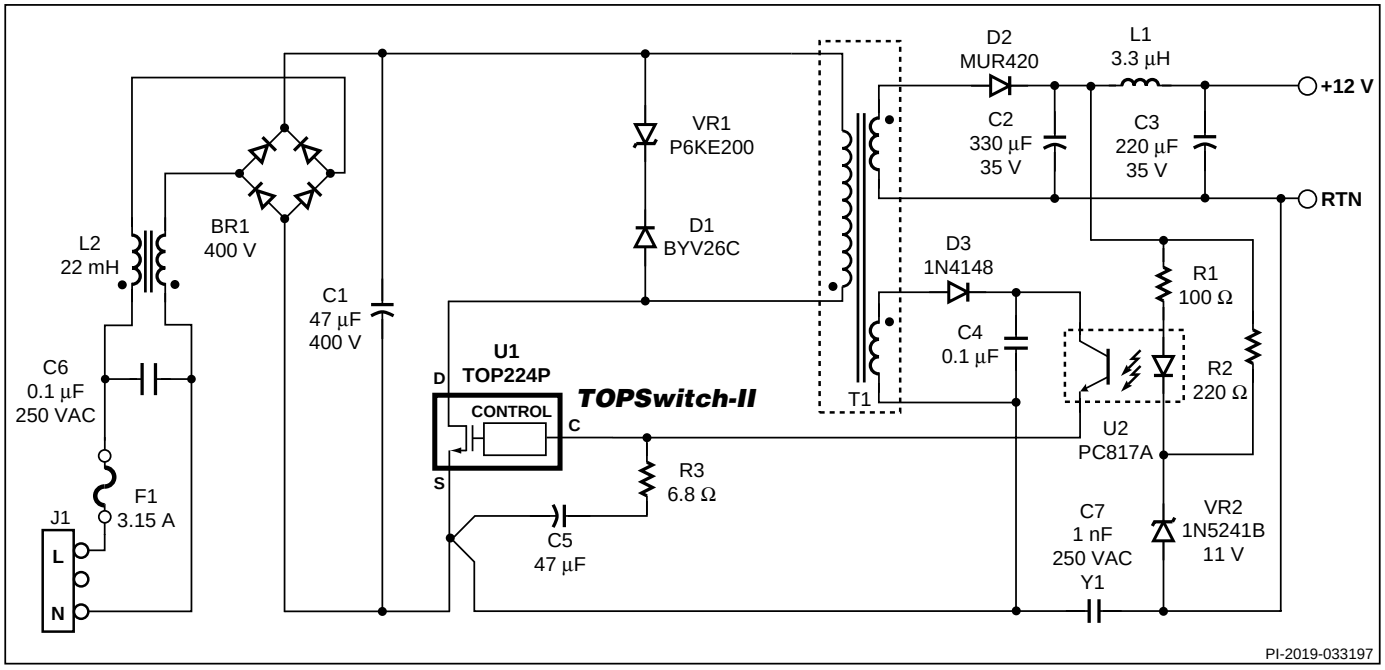


Figure 8. Schematic Diagram of a 20 W Universal Input TOPSwitch-II Power Supply using an 8 lead PDIP.

20 W Universal Supply using 8 Lead PDIP

Figure 8 shows a 12 V, 20 W secondary regulated flyback power supply using the TOP224P in an eight lead PDIP package and operating from universal 85 to 265 VAC input voltage. This example demonstrates the advantage of the higher power 8 pin leadframe used with the *TOPSwitch-II* family. This low cost package transfers heat directly to the board through six source pins, eliminating the heatsink and the associated cost. Efficiency is typically 80% at low line input. Output voltage is directly sensed by optocoupler U2 and Zener diode VR2. The output voltage is determined by the Zener diode (VR2) voltage and the voltage drops across the optocoupler (U2) LED and resistor R1. Other output voltages are possible by adjusting the transformer turns ratio and value of Zener diode VR2.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated *TOPSwitch-II* high-voltage MOSFET. D1 and VR1 clamp leading-edge voltage spikes caused by transformer leakage inductance. The power secondary winding is rectified and filtered by D2, C2, L1, and C3 to create the 12 V output voltage. R2 and VR2 provide a slight pre-load on the 12 V output to improve load regulation at light loads. The bias winding is rectified and filtered by D3 and C4 to create a *TOPSwitch* bias voltage. L2 and Y1-safety capacitor C7 attenuate common mode emission currents caused by high voltage switching waveforms on the DRAIN side of the primary winding and the primary to secondary capacitance. Leakage inductance of L2 with C1 and C6 attenuates differential-mode emission currents caused by the fundamental and harmonics of the trapezoidal or triangular primary current waveform. C5 filters internal MOSFET gate drive charge current spikes on the CONTROL pin, determines the auto-restart frequency, and together with R1 and R3, compensates the control loop.

Key Application Considerations

General Guidelines

- Keep the SOURCE pin length very short. Use a Kelvin connection to the SOURCE pin for the CONTROL pin bypass capacitor. Use single point grounding techniques at the SOURCE pin as shown in Figure 9.

- Minimize peak voltage and ringing on the DRAIN voltage at turn-off. Use a Zener or TVS Zener diode to clamp the drain voltage below the breakdown voltage rating of *TOPSwitch* under all conditions, including start-up and overload. The maximum recommended clamp Zener voltage for the TOP2XX series is 200 V and the corresponding maximum reflected output voltage on the primary is 135 V. Please see Step 4: AN-16 in the 1996-97 Data Book and Design Guide or on our Web site.

- The transformer should be designed such that the rate of change of drain current due to transformer saturation is within the absolute maximum specification (ΔI_D in 100 ns before turn off as shown in Figure 13). As a guideline, for most common transformer cores, this can be achieved by maintaining the Peak Flux Density (at maximum I_{LIMIT} current) below 4200 Gauss (420 mT). The transformer spreadsheets Rev. 2.1 (or later) for continuous and Rev.1.0 (or later) for discontinuous conduction mode provide the necessary information.

- Do not plug *TOPSwitch* into a “hot” IC socket during test. External CONTROL pin capacitance may be charged to excessive voltage and cause *TOPSwitch* damage.

- While performing *TOPSwitch* device tests, do not exceed maximum CONTROL pin voltage of 9 V or maximum CONTROL pin current of 100 mA.

- Under some conditions, externally provided bias or supply current driven into the CONTROL pin can hold the *TOPSwitch* in one of the 8 auto-restart cycles indefinitely and prevent starting. To avoid this problem when doing bench evaluations, it is recommended that the V_C power supply be turned on before the DRAIN voltage is applied. *TOPSwitch* can also be reset by shorting the CONTROL pin to the SOURCE pin momentarily.

- CONTROL pin currents during auto-restart operation are much lower at low input voltages (< 36 V) which increases the auto-restart cycle time (see the I_C vs. DRAIN Voltage Characteristic curve).

- Short interruptions of AC power may cause *TOPSwitch* to enter the 8-count auto-restart cycle before starting again. This is because the input energy storage capacitors are not completely discharged and the CONTROL pin capacitance has not discharged below the internal power-up reset voltage.

- In some cases, minimum loading may be necessary to keep a lightly loaded or unloaded output voltage within the desired range due to the minimum ON-time.

Replacing*TOPSwitch* with *TOPSwitch-II*

There is no external latching shutdown function in *TOPSwitch-II*. Otherwise, the functionality of the *TOPSwitch-II* devices is same as that of the *TOPSwitch* family. However, **before considering *TOPSwitch-II* as a 'drop in' replacement in an existing *TOPSwitch* design, the design should be verified as described below.**

The new *TOPSwitch-II* family offers more power capability than the original *TOPSwitch* family for the same MOSFET $R_{DS(ON)}$. Therefore, the original *TOPSwitch* design must be reviewed to make sure that the selected *TOPSwitch-II* replacement device and other primary components are not over stressed under abnormal conditions.

The following verification steps are recommended:

- Check the transformer design to make sure that it meets the ΔI_D specification as outlined in the General Guidelines section above.

- Thermal: Higher power capability of the *TOPSwitch-II* would in many instances allow use of a smaller MOSFET device (higher $R_{DS(ON)}$) for reduced cost. This may affect *TOPSwitch* power dissipation and power supply efficiency. Therefore thermal performance of the power supply must be verified with the selected *TOPSwitch-II* device.

- Clamp Voltage: Reflected and Clamp voltages should be verified not to exceed recommended maximums for the TOP2XX Series: 135 V Reflected/200 V Clamp. Please see Step 4: AN-16 in the Data Book and Design Guide and readme.txt file attached to the transformer design spreadsheets.

- Agency Approval: Migrating to *TOPSwitch-II* may require agency re-approval.

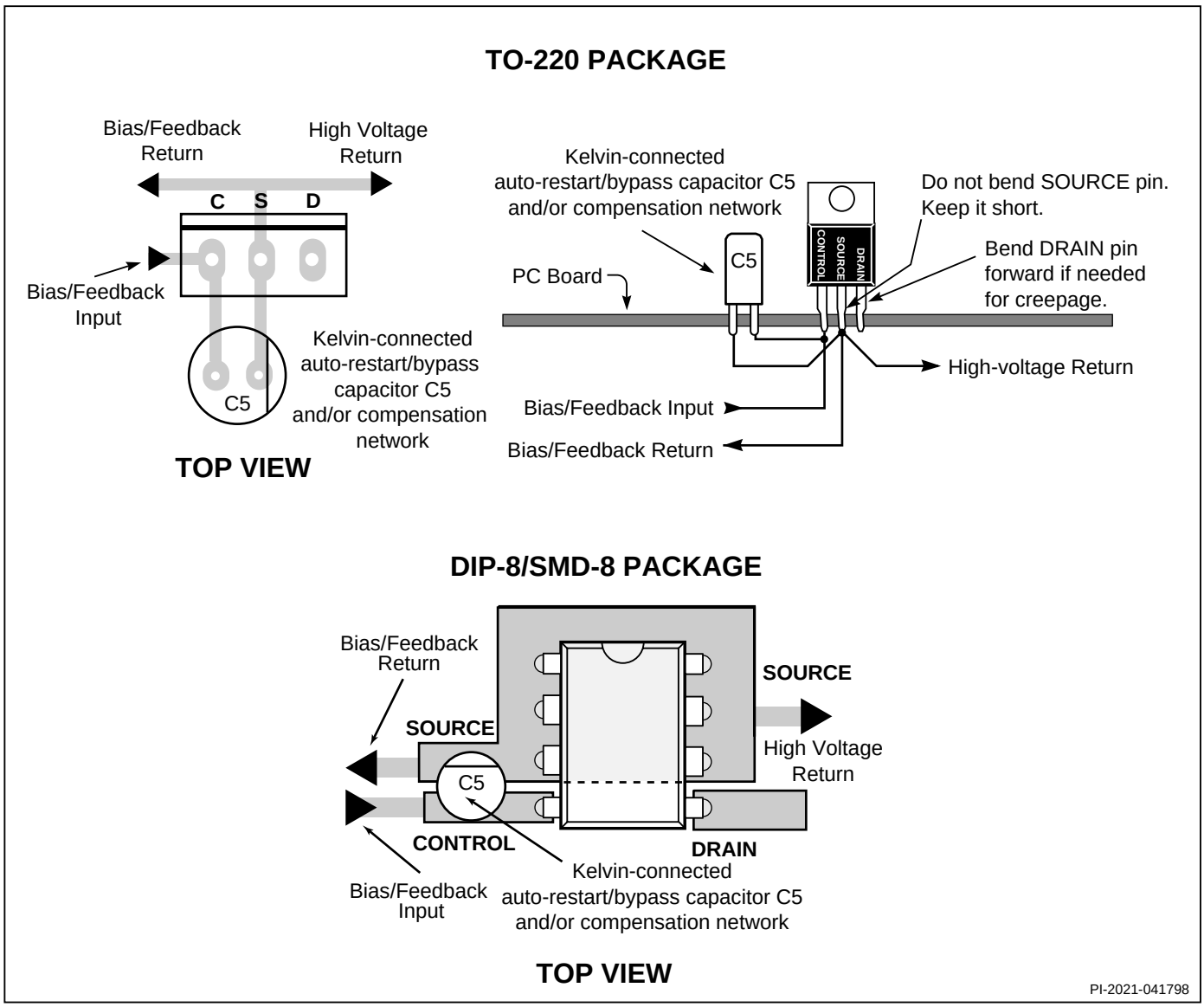


Figure 9. Recommended TOPSwitch Layout.

Design Tools

The following tools available from Power Integrations greatly simplify *TOPSwitch* based power supply design.

- Data Book and Design Guide includes extensive application information
- Excel Spreadsheets for Transformer Design - **Use of this tool is strongly recommended for all *TOPSwitch* designs.**
- Reference design boards – Production viable designs that are assembled and tested.

All data sheets, application literature and up-to-date versions of the Transformer Design Spreadsheets can be downloaded from our Web site at ***www.powerint.com***. A diskette of the Transformer Design Spreadsheets may also be obtained by sending in the completed form provided at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

DRAIN Voltage ..... -0.3 to 700 V
DRAIN Current Increase (ΔI_D) in 100 ns except during blanking time ..... 0.1 x $I_{LIMIT(MAX)}$ (2)
CONTROL Voltage ..... - 0.3 V to 9 V
CONTROL Current ..... 100 mA
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature(3) ..... -40 to 150 °C
Lead Temperature(4) ..... 260 °C
Thermal Impedance: Y Package (θ_{JA})(5) .....70 °C/W
(θ_{JC})(6) .....2 °C/W
P/G Package:
(θ_{JA}) .....45 °C/W(7); 35 °C/W(8)
(θ_{JC})(6).....11 °C/W

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Related to transformer saturation – see Figure 13.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Free standing with no heatsink.
6. Measured at tab closest to plastic interface or SOURCE pin.
7. Soldered to 0.36 sq. inch (232 mm^2), 2 oz. (610 gm/m^2) copper clad.
8. Soldered to 1 sq. inch (645 mm^2), 2 oz. (610 gm/m^2) copper clad.

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V; T_J = -40 to 125 °C		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	I_C = 4 mA, T_J = 25 °C		90	100	110	kHz
Maximum Duty Cycle	D_{MAX}	$I_C = I_{CD1}$ + 0.4 mA, See Figure 10		64	67	70	%
Minimum Duty Cycle	D_{MIN}	I_C = 10 mA, See Figure 10		0.7	1.7	2.7	%
PWM Gain		I_C = 4 mA, T_J = 25 °C See Figure 4		-21	-16	-11	%/mA
PWM Gain Temperature Drift		See Note A			-0.05		%/mA/°C
External Bias Current	I_B	See Figure 4		0.8	2.0	3.3	mA
Dynamic Impedance	Z_C	I_C = 4 mA, T_J = 25 °C See Figure 11		10	15	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	I_C	T_J = 25 °C	V_C = 0 V	-2.4	-1.9	-1.2	mA
			V_C = 5 V	-2	-1.5	-0.8	
Charging Current Temperature Drift		See Note A			0.4		%/°C

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V; T_J = -40 to 125 °C		Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART (cont.)							
Auto-restart Threshold Voltage	$V_{C(AR)}$	S1 open			5.7		V
UV Lockout Threshold Voltage		S1 open		4.4	4.7	5.0	V
Auto-restart Hysteresis Voltage		S1 open		0.6	1.0		V
Auto-restart Duty Cycle		S1 open	TOP221-222	2	5	9	%
			TOP223-227	2	5	8	
Auto-restart Frequency		S1 open			1.2		Hz
CIRCUIT PROTECTION							
Self-protection Current Limit	I_{LIMIT}	di/dt = 40 mA/µs, T_J = 25 °C	TOP221Y	0.23	0.25	0.28	A
			TOP221P or G				
		di/dt = 80 mA/µs, T_J = 25 °C	TOP222Y	0.45	0.50	0.55	
			TOP222P or G				
		di/dt = 160 mA/µs, T_J = 25 °C	TOP223Y	0.90	1.00	1.10	
			TOP223P or G				
		di/dt = 240 mA/µs, T_J = 25 °C	TOP224Y	1.35	1.50	1.65	
			TOP224P or G				
		di/dt = 320 mA/µs, T_J = 25 °C	TOP225Y	1.80	2.00	2.20	
		di/dt = 400 mA/µs, T_J = 25 °C	TOP226Y	2.25	2.50	2.75	
		di/dt = 480 mA/µs, T_J = 25 °C	TOP227Y	2.70	3.00	3.30	
Initial Current Limit	I_{INIT}	See Figure 12 T_J = 25 °C	≤ 85 VAC (Rectified Line Input)	0.75 x $I_{LIMIT(MIN)}$			A
			265 VAC (Rectified Line Input)	0.6 x $I_{LIMIT(MIN)}$			
Leading Edge Blanking Time	t_{LEB}	I_C = 4 mA, T_J = 25 °C			180		ns

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V; T_J = -40 to 125 °C		Min	Typ	Max	Units
CIRCUIT PROTECTION (cont.)							
Current Limit Delay	t_{ILD}	I_C = 4 mA			100		ns
Thermal Shutdown Temperature		I_C = 4 mA		125	135		°C
Power-up Reset Threshold Voltage	$V_{C(RESET)}$	S2 open		2.0	3.3	4.3	V
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	TOP221 I_D = 25 mA	T_J = 25 °C		31.2	36.0	Ω
			T_J = 100 °C		51.4	60.0	
		TOP222 I_D = 50 mA	T_J = 25 °C		15.6	18.0	
			T_J = 100 °C		25.7	30.0	
		TOP223 I_D = 100 mA	T_J = 25 °C		7.8	9.0	
			T_J = 100 °C		12.9	15.0	
		TOP224 I_D = 150 mA	T_J = 25 °C		5.2	6.0	
			T_J = 100 °C		8.6	10.0	
		TOP225 I_D = 200 mA	T_J = 25 °C		3.9	4.5	
			T_J = 100 °C		6.4	7.5	
		TOP226 I_D = 250 mA	T_J = 25 °C		3.1	3.6	
			T_J = 100 °C		5.2	6.0	
		TOP227 I_D = 300 mA	T_J = 25 °C		2.6	3.0	
			T_J = 100 °C		4.3	5.0	
OFF-State Current	I_{DSS}	See Note B V_{DS} = 560 V, T_A = 125 °C				250	µA
Breakdown Voltage	BV_{DSS}	See Note B I_D = 100 µA, T_A = 25 °C		700			V
Rise Time	t_R	Measured in a Typical Flyback Converter Application.			100		ns
Fall Time	t_F				50		ns

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 14 SOURCE = 0 V; T_J = -40 to 125 °C		Min	Typ	Max	Units
OUTPUT (cont.)							
DRAIN Supply Voltage		See Note C		36			V
Shunt Regulator Voltage	$V_{C(SHUNT)}$	I_C = 4 mA		5.5	5.7	6.0	V
Shunt Regulator Temperature Drift					±50		ppm/°C
CONTROL Supply/ Discharge Current	I_{CD1}	Output MOSFET Enabled	TOP221-224	0.6	1.2	1.6	mA
			TOP225-227	0.7	1.4	1.8	
	I_{CD2}	Output MOSFET Disabled		0.5	0.8	1.1	

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. The breakdown voltage and leakage current measurements can be accomplished as shown in Figure 15 by using the following sequence:

i. The curve tracer should initially be set at 0 V. The base output should be adjusted through a voltage sequence of 0 V, 6.5 V, 4.3 V, and 6.5 V, as shown. The base current from the curve tracer should not exceed 100 mA. This CONTROL pin sequence interrupts the Auto-restart sequence and locks the *TOPSwitch* internal MOSFET in the OFF State.

ii. The breakdown and the leakage measurements can now be taken with the curve tracer. The maximum voltage from the curve tracer must be limited to 700 V under all conditions.

C. It is possible to start up and operate *TOPSwitch* at DRAIN voltages well below 36 V. However, the CONTROL pin charging current is reduced, which affects start-up time, auto-restart frequency, and auto-restart duty cycle. Refer to the characteristic graph on CONTROL pin charge current (I_C) vs. DRAIN voltage for low voltage operation characteristics.

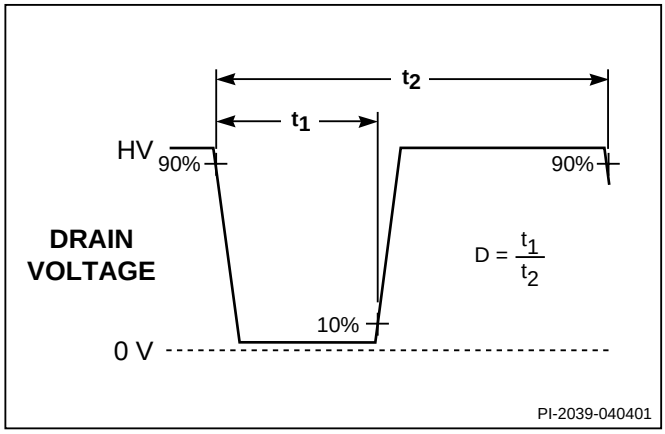


Figure 10. TOPSwitch Duty Cycle Measurement.

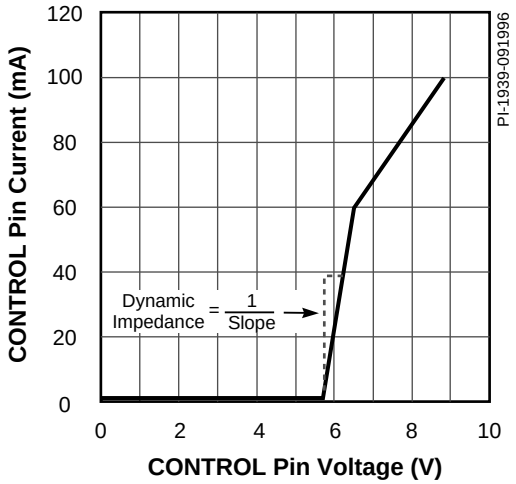


Figure 11. TOPSwitch CONTROL Pin I-V Characteristic.

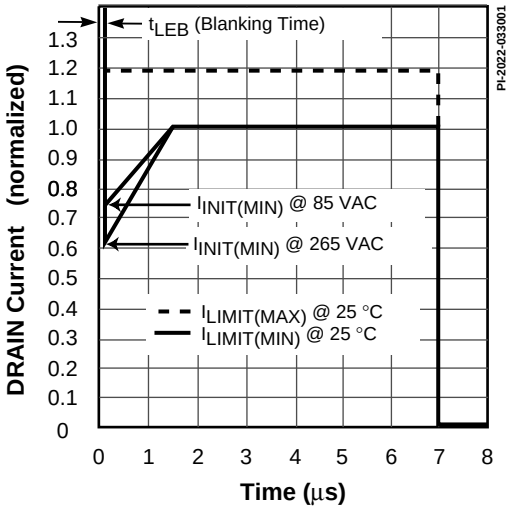


Figure 12. Self-protection Current Limit Envelope.

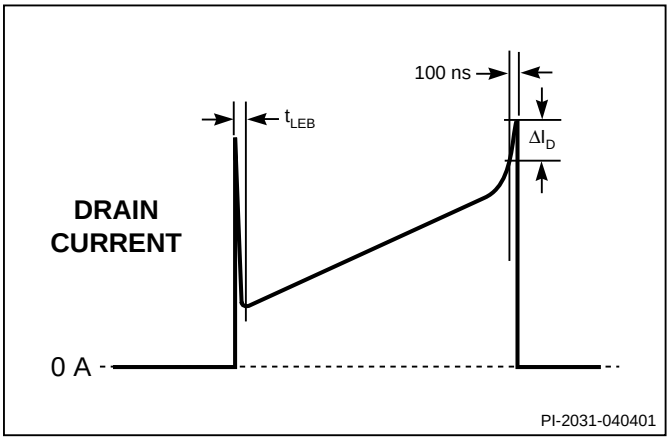
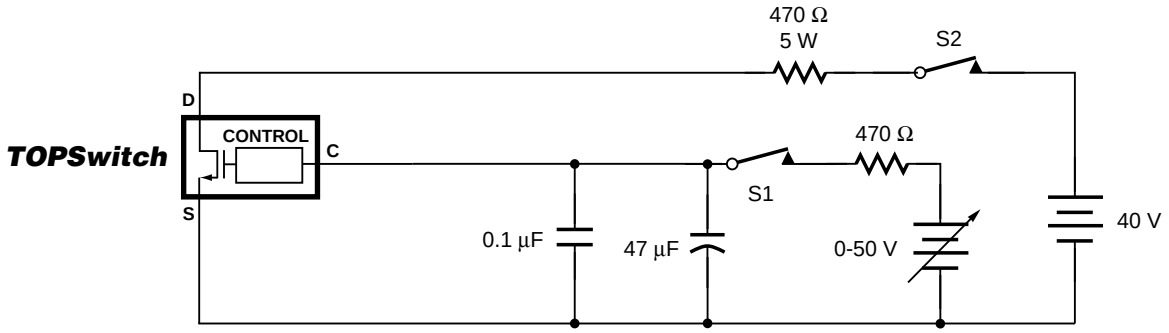


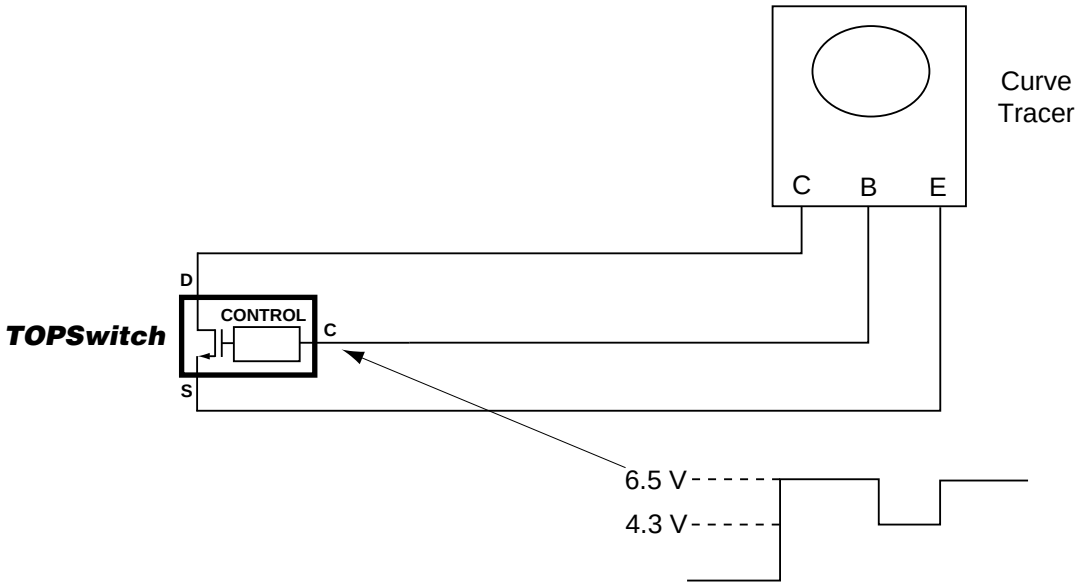
Figure 13. Example of ΔI_D on Drain Current Waveform with Saturated Transformer.



NOTES: 1. This test circuit is not applicable for current limit or output characteristic measurements.
2. For P package, short all SOURCE and SOURCE (HV RTN) pins together.

PI-1964-110696

Figure 14. TOPSwitch General Test Circuit.



NOTE: This CONTROL pin sequence interrupts the Auto-restart sequence and locks the *TOPSwitch* internal MOSFET in the OFF State.

PI-2109-040401

Figure 15. Breakdown Voltage and Leakage Current Measurement Test Circuit.

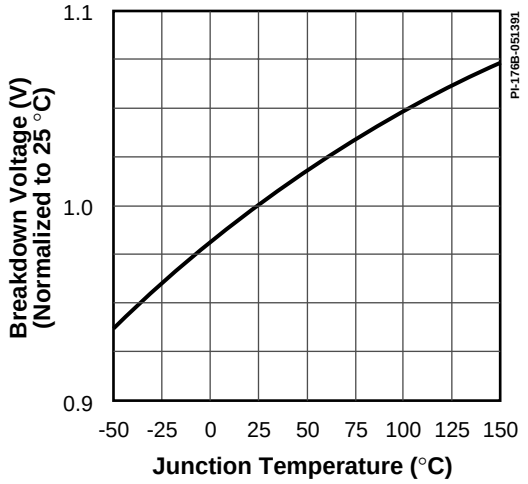
BENCH TEST PRECAUTIONS FOR EVALUATION OF ELECTRICAL CHARACTERISTICS

The following precautions should be followed when testing *TOPSwitch* by itself outside of a power supply. The schematic shown in Figure 14 is suggested for laboratory testing of *TOPSwitch*.

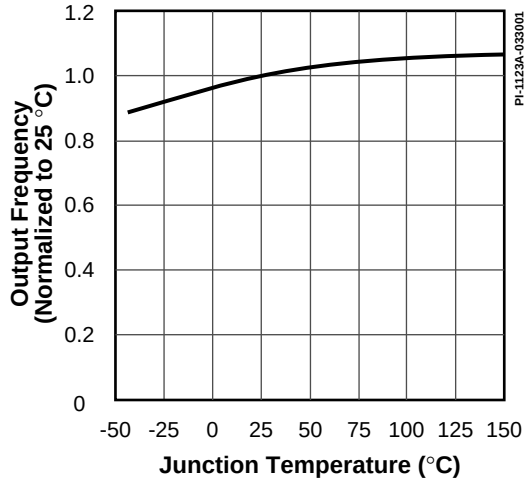
When the DRAIN supply is turned on, the part will be in the Auto-restart mode. The CONTROL pin voltage will be oscillating at a low frequency from 4.7 to 5.7 V and the DRAIN is turned on every eighth cycle of the CONTROL pin oscillation. If the CONTROL pin power supply is turned on while in this Auto-restart mode, there is only a 12.5% chance that the control pin oscillation will be in the correct state (DRAIN active state) so that the continuous DRAIN voltage waveform may be observed. It is recommended that the V_C power supply be turned on first and the DRAIN power supply second if continuous drain voltage waveforms are to be observed. The 12.5% chance of being in the correct state is due to the 8:1 counter. Temporarily shorting the CONTROL pin to the SOURCE pin will reset *TOPSwitch*, which then will come up in the correct state.

Typical Performance Characteristics

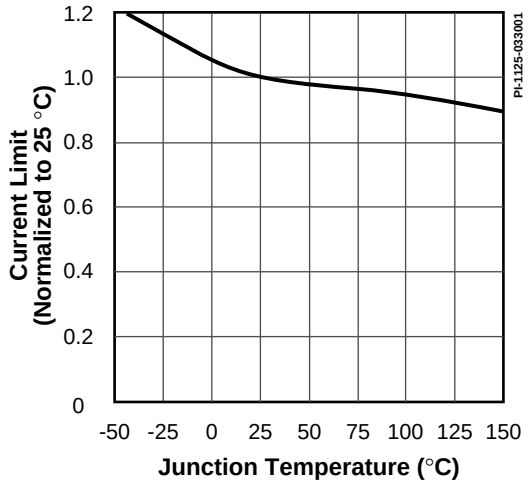
BREAKDOWN vs. TEMPERATURE



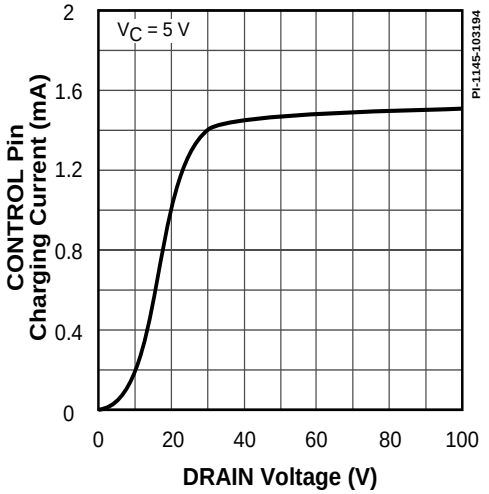
FREQUENCY vs. TEMPERATURE



CURRENT LIMIT vs. TEMPERATURE

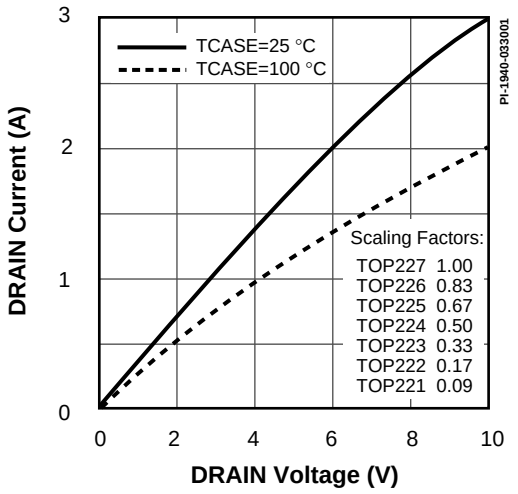


I_C vs. DRAIN VOLTAGE

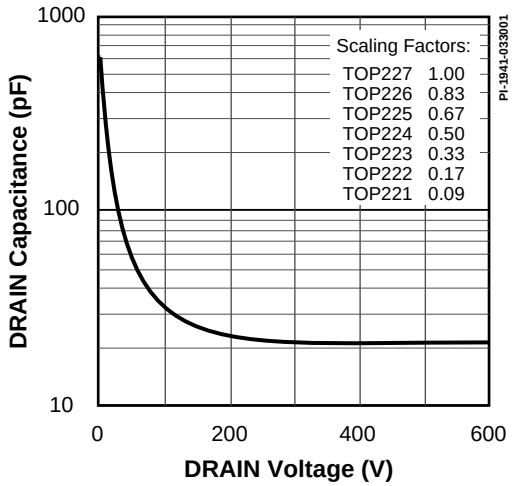


Typical Performance Characteristics (cont.)

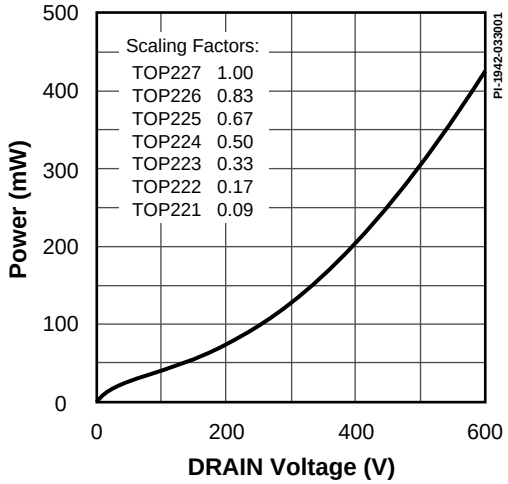
OUTPUT CHARACTERISTICS



C_{OSS} vs. DRAIN VOLTAGE

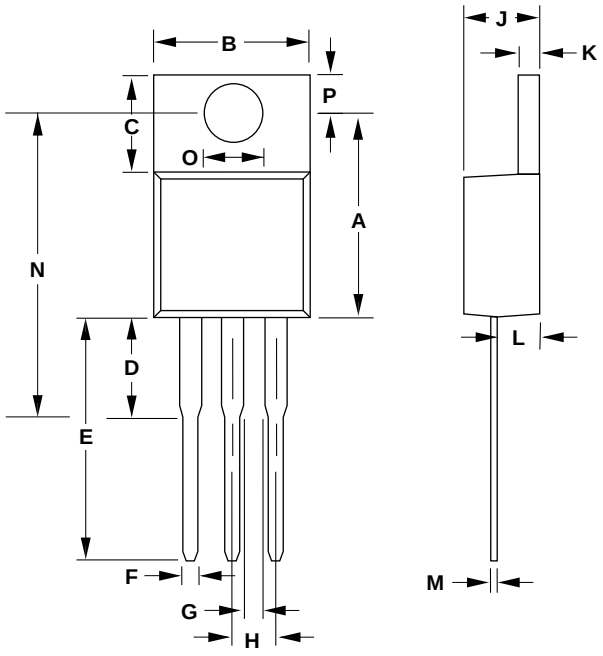


DRAIN CAPACITANCE POWER



TO-220/3

DIM	inches	mm
A	.460-.480	11.68-12.19
B	.400-.415	10.16-10.54
C	.236-.260	5.99-6.60
D	.240 - REF.	6.10 - REF.
E	.520-.560	13.21-14.22
F	.028-.038	.71-.97
G	.045-.055	1.14-1.40
H	.090-.110	2.29-2.79
J	.165-.185	4.19-4.70
K	.045-.055	1.14-1.40
L	.095-.115	2.41-2.92
M	.015-.020	.38-.51
N	.705-.715	17.91-18.16
O	.146-.156	3.71-3.96
P	.103-.113	2.62-2.87



Notes:
1. Package dimensions conform to JEDEC specification TO-220 AB for standard flange mounted, peripheral lead package; .100 inch lead spacing (Plastic) 3 leads (issue J, March 1987)
2. Controlling dimensions are inches.
3. Pin numbers start with Pin 1, and continue from left to right when viewed from the top.
4. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
5. Position of terminals to be measured at a position .25 (6.35 mm) from the body.
6. All terminals are solder plated.

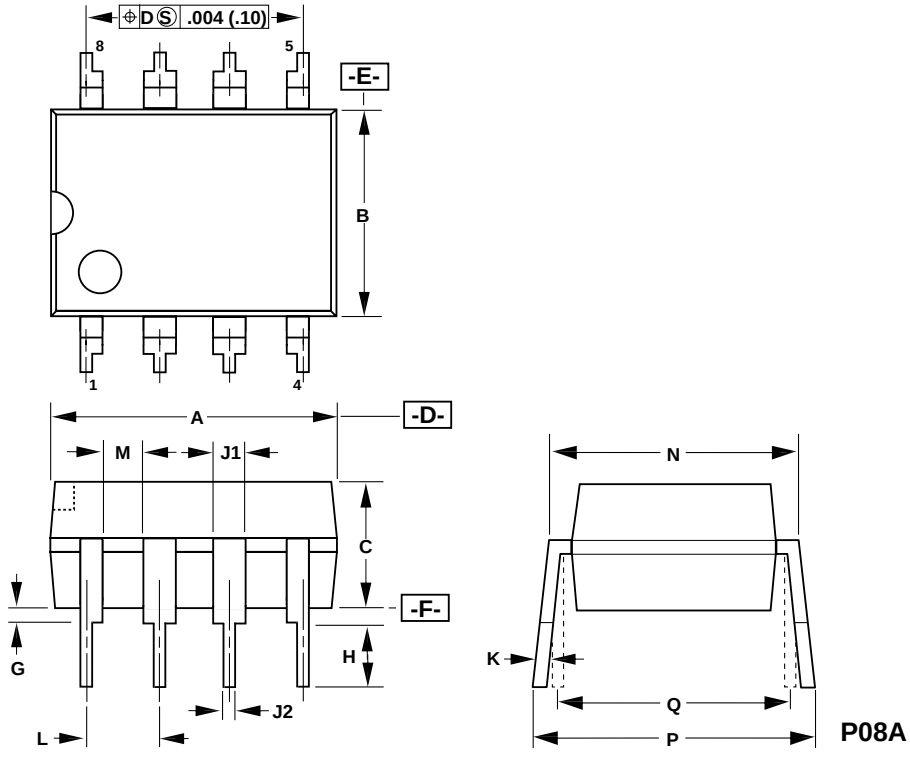
Y03A

PI-1848-040901

DIP-8

DIM	inches	mm
A	0.370-0.385	9.40-9.78
B	0.245-0.255	6.22-6.48
C	0.125-0.135	3.18-3.43
G	0.015-0.040	0.38-1.02
H	0.120-0.135	3.05-3.43
J1	0.060 (NOM)	1.52 (NOM)
J2	0.014-0.022	0.36-0.56
K	0.010-0.012	0.25-0.30
L	0.090-0.110	2.29-2.79
M	0.030 (MIN)	0.76 (MIN)
N	0.300-0.320	7.62-8.13
P	0.300-0.390	7.62-9.91
Q	0.300 BSC	7.62 BSC

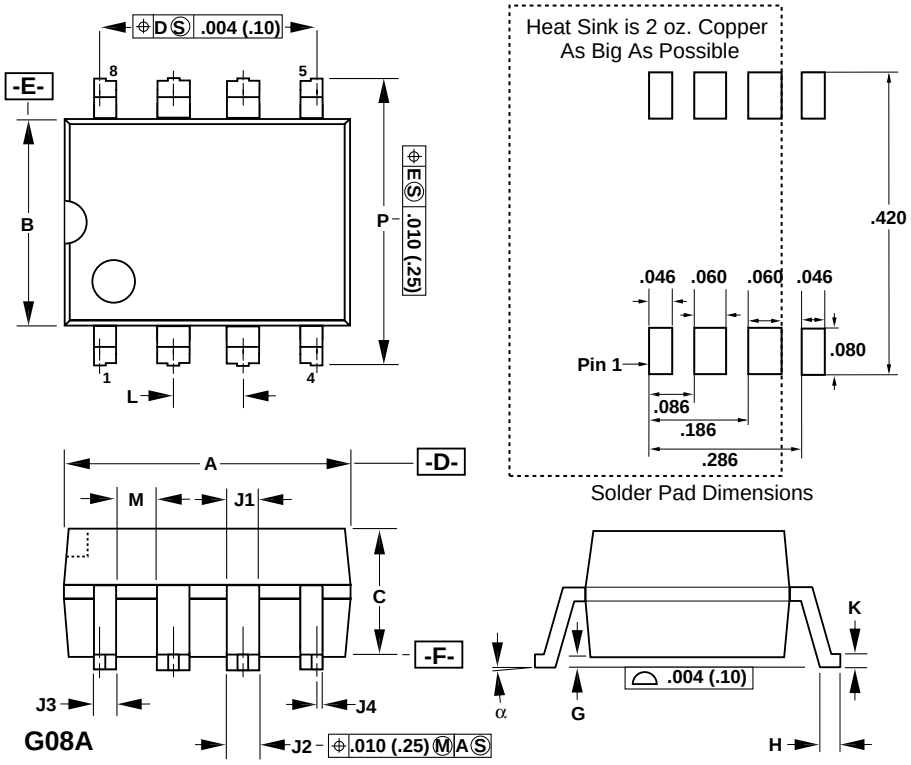
Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85)..
2. Controlling dimensions are inches.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums on the molded body.



P08A

PI-2076-040901

SMD-8



DIM	inches	mm
A	0.370-0.385	9.40-9.78
B	0.245-0.255	6.22-6.48
C	0.125-0.135	3.18-3.43
G	0.004-0.012	0.10-0.30
H	0.036-0.044	0.91-1.12
J1	0.060 (NOM)	1.52 (NOM)
J2	0.048-0.053	1.22-1.35
J3	0.032-0.037	0.81-0.94
J4	0.007-0.011	0.18-0.28
K	0.010-0.012	0.25-0.30
L	0.100 BSC	2.54 BSC
M	0.030 (MIN)	0.76 (MIN)
P	0.372-0.388	9.45-9.86
α	0-8°	0-8°

Notes:

1. **Package dimensions conform to JEDEC specification MS-001-AB (issue B, 7/85) except for lead shape and size.**
2. **Controlling dimensions are inches.**
3. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
4. **D, E and F are reference datums on the molded body.**

PI-2077-042601

Revision	Notes	Date
C	-	12/97
D	1) Updated package references. 2) Corrected Spelling. 3) Corrected Storage Temperature θ_{JC} and updated nomenclature in parameter table. 4) Added G package references to Self-Protection Current Limit parameter. 5) Corrected font sizes in figures.	7/01

For the latest updates, visit our Web site: ***www.powerint.com***
Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein, nor does it convey any license under its patent rights or the rights of others.

The PI Logo, ***TOPSwitch***, ***TinySwitch*** and ***EcoSmart*** are registered trademarks of Power Integrations, Inc.
©Copyright 2001, Power Integrations, Inc.

WORLD HEADQUARTERS AMERICAS
Power Integrations, Inc.
5245 Hellyer Avenue
San Jose, CA 95138 USA
Main: +1 408-414-9200
Customer Service:
Phone: +1 408-414-9665
Fax: +1 408-414-9765
e-mail: usasales@powerint.com

EUROPE & AFRICA
Power Integrations (Europe) Ltd.
Centennial Court
Easthampstead Road
Bracknell
Berkshire, RG12 1YQ
United Kingdom
Phone: +44-1344-462-300
Fax: +44-1344-311-732
e-mail: eurosales@powerint.com

TAIWAN
Power Integrations
International Holdings, Inc.
17F-3, No. 510
Chung Hsiao E. Rd.,
Sec. 5,
Taipei, Taiwan 110, R.O.C.
Phone: +886-2-2727-1221
Fax: +886-2-2727-1223
e-mail: taiwansales@powerint.com

CHINA
Power Integrations
International Holdings, Inc.
Rm# 1705, Bao Hua Bldg.
1016 Hua Qiang Bei Lu
Shenzhen, Guangdong 518031
China
Phone: +86-755-367-5143
Fax: +86-755-377-9610
e-mail: chinasales@powerint.com

KOREA
Power Integrations
International Holdings, Inc.
Rm# 402, Handuk Building
649-4 Yeoksam-Dong,
Kangnam-Gu,
Seoul, Korea
Phone: +82-2-568-7520
Fax: +82-2-568-7474
e-mail: koreasales@powerint.com

JAPAN
Power Integrations, K.K.
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama 2-Chome
Kohoku-ku, Yokohama-shi
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

INDIA (Technical Support)
Innovatech
#1, 8th Main Road
Vasanthnagar
Bangalore, India 560052
Phone: +91-80-226-6023
Fax: +91-80-228-9727
e-mail: indiasales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760