Preliminary Data Sheet, Version 1.3, November 2003

ICE 1QS01

Controller for Quasiresonant Switch Mode Power Supplies Supporting Low Power Standby and Power Factor Correction

Power Management & Supply



Never stop thinking.

ICE1QS01 Revision History: Current Version: 2003-11-28		
Previous Version: 2002-08-12		
Page 3 (in previous version)	Page 3 (in current version)	Ordering Codes shortened
Page 15 (in previous version)	Page 16 (in current version)	Subjects (major changes since last revision) ICCL, ICCH, VCCON changed
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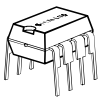
Information

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Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in

Controller for Switch Mode Power Supplies Supporting Low Power Standby and Power Factor Correction (PFC)



P-DIP-8-4

P-DIP-8-4



P-DSO-8-3

P-DSO-8-3

Features

- Line Current Consumption with PFC
- Standby Input Power < 1 W
- Stable Standby Frequency
- Low Power Consumption
- Very Low Start-up Current
- Soft-Start for noiseless Start-up
- Standby Burst Mode with and without Control Signal for lowered Output Voltages
- Digital Frequency Reduction in small Steps at Decreasing Load
- Over- and Undervoltage Lockout
- Switch Off at Mains Undervoltage
- Mains Voltage Dependent Fold Back Point Correction
- Ringing Suppression Time Controlled from Output Voltage
- Easy Design In
- Free usable Fault Comparator

Functional Description

The ICE1QS01 is optimized to control free running flyback converters with and without Power Factor Correction (with PFC Charge Pump).

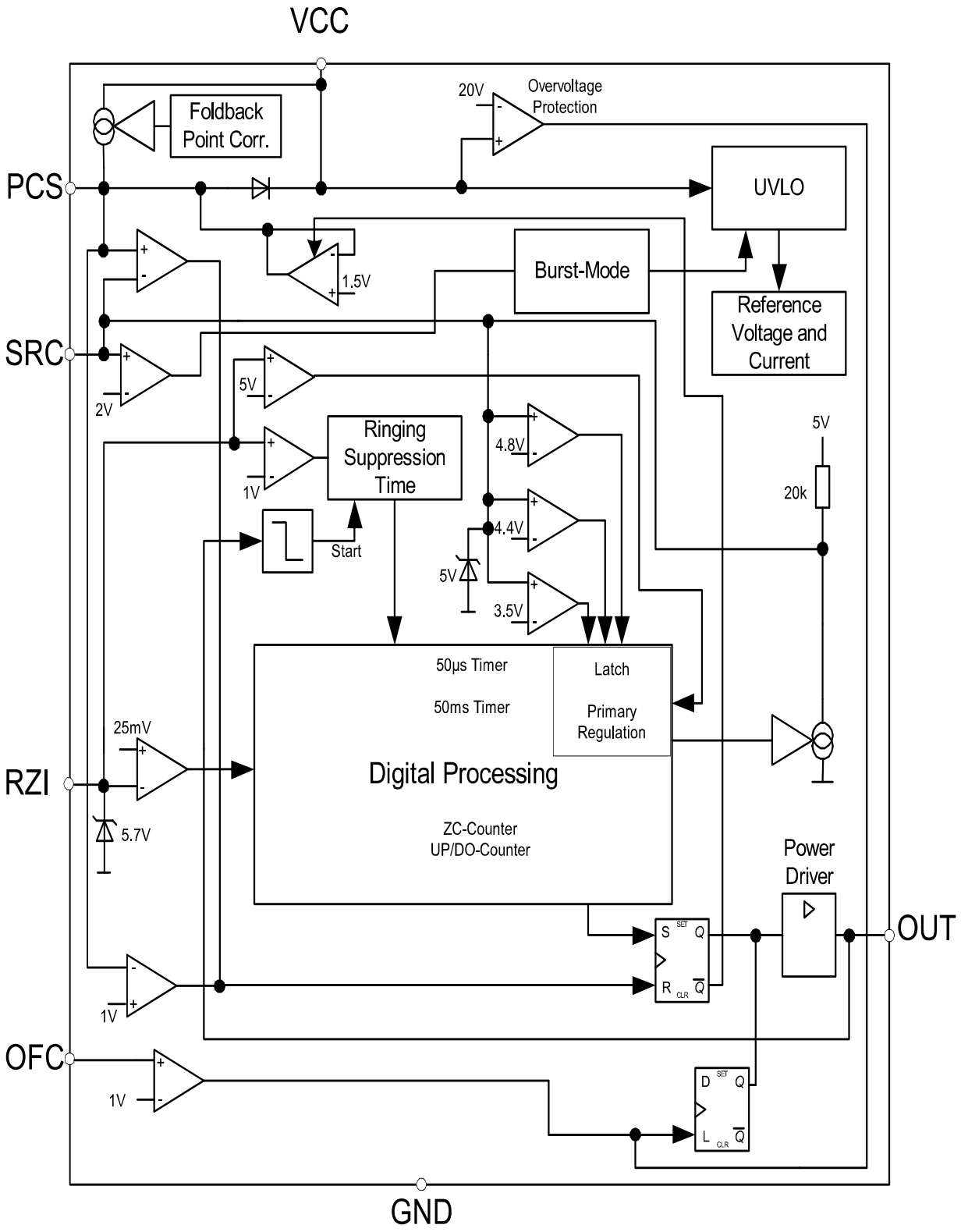
The switching frequency is reduced in small steps with decreasing load towards a minimum of 20 kHz in standby mode. This function is performed by a digital circuit to avoid any jitter also with periodically pulsed loads. To provide extremely low power consumption at light loads, this device can be switched into Standby Burst Mode. This is also possible without standby control signal (for adapter application).

Additionally, the start up current is very low. To avoid switching stresses of the power devices, the power transistor is always switched on at minimum voltage. The device has several protection functions: V_{CC} over- and undervoltage, mains undervoltage and current limiting. Regulation can be done by using the internal error amplifier or an opto coupler feedback. The output driver is ideally suited for driving a power MOSFET.

The ICE1QS01 is suited for TV-sets, VCR- sets, SAT- receivers and other consumer applications in the power range from 0 to app. 300 W.

Type	Ordering Code	Package
ICE1QS01	Q67040-S4558	P-DIP-8
ICE1QS01G	Q67040-S4559	P-DSO-8

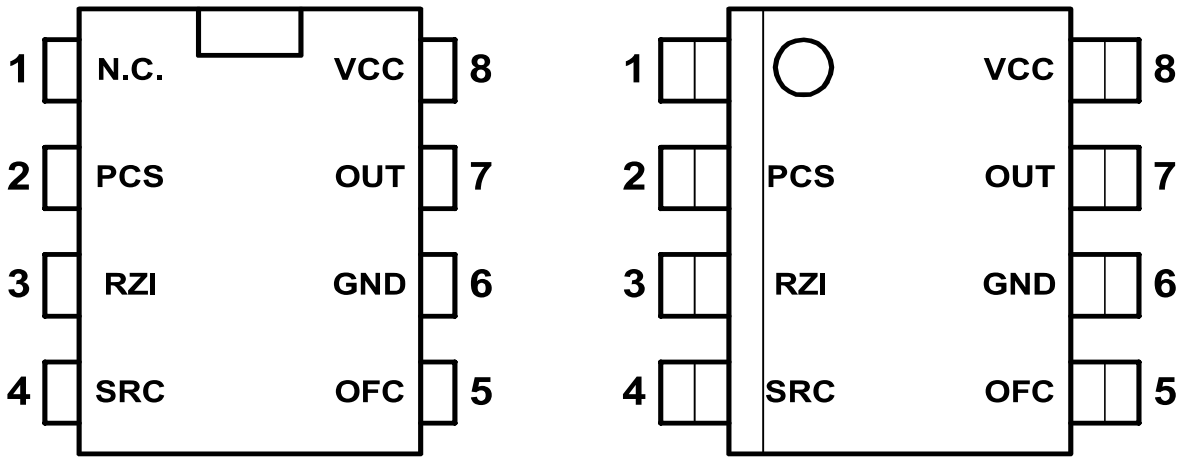
Block Diagram



Pinning

Pin	Symbol	Function
1	N.C.	
2	PCS	Primary Current Simulation
3	RZI	Regulation and Zero Crossing Input
4	SRC	Soft-Start and Regulation Capacitor
5	OFC	Overvoltage Fault Comparator
6	GND	Ground
7	OUT	Output
8	VCC	Supply Voltage

Pin Configuration (top view)



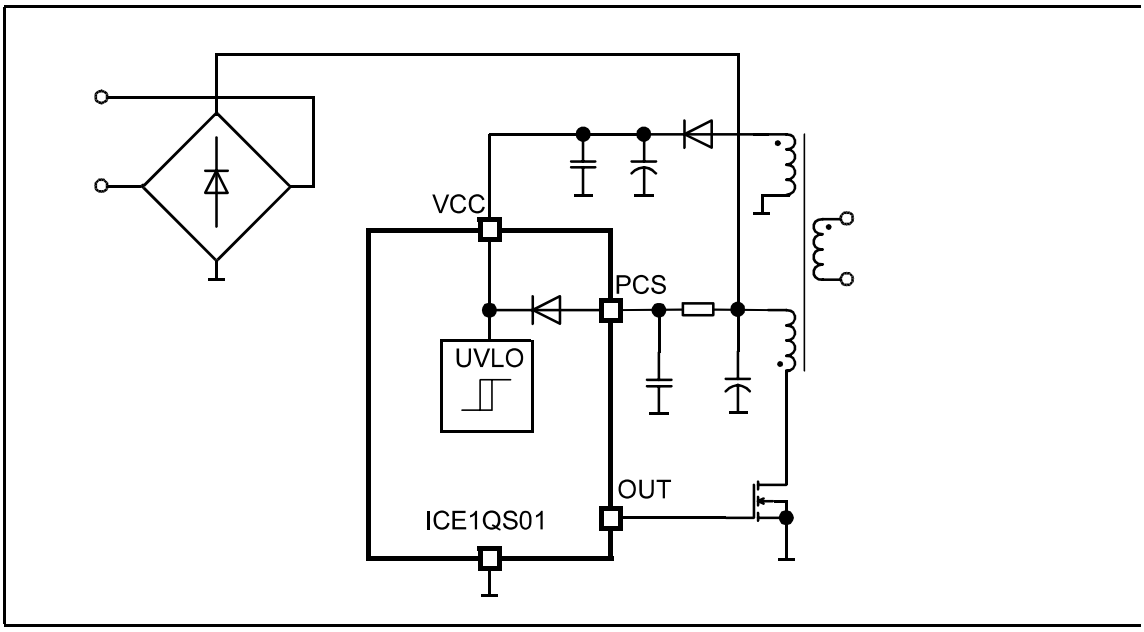
Functional Description

Start up

An internal start up diode is connected between pin PCS and pin V_{CC}. Start up current is provided via this diode if V_{PCS} is higher than V_{CC} + V_{BE} (V_{BE} = Base-Emitter-Voltage).

During start up the internal reference of the IC is shut off and current consumption is about 50uA. There is only the start up circuitry working which determines the V_{CCon} threshold. Gate driver OUT is switched to low. An active shut down circuitry ensures that OUT is held below the MOS gate threshold when the IC is in start up mode.

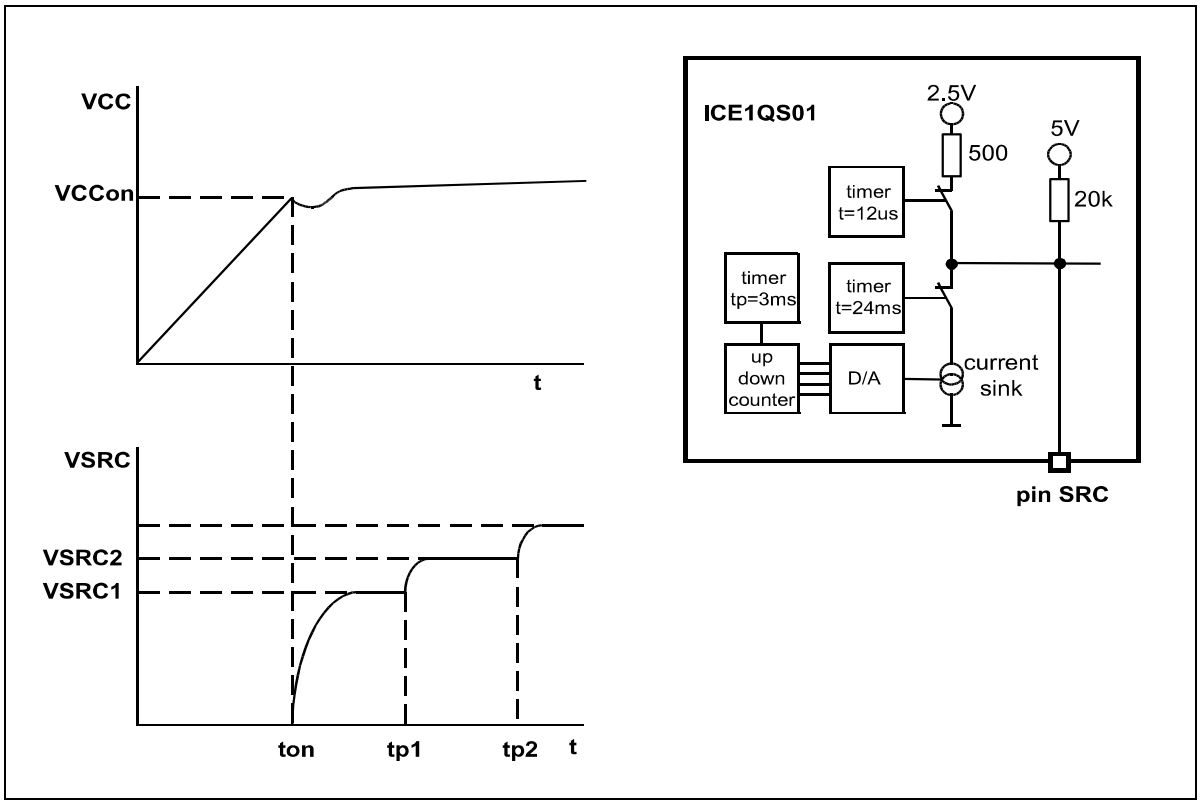
Block Diagram: Start Up



Soft start

The internal reference of the IC is switched on when V_{CC} exceeds the V_{CCon} threshold. The IC begins to work with soft start mode. Soft start is realized with an internal soft start resistor, an internal current sink, a current source and the external feedback capacitor connected at pin SRC. The internal resistor is connected between the internal voltage reference and pin SRC. The current sink is connected between pin SRC and GND. The value of the current is set with a timer. Immediately after the IC is switched on the capacitor C_{SRC} is charged with a current source up to 2.5V. This current source is switched off 12 µsec after beginning of soft start. The current value of the current sink is set with a timer. Every three msec the current of the current sink is reduced and so V_{SRC} can increase stepwise. The soft start is finished 24 msec after the IC is switched on. At the end of the soft start the current sink is switched off.

Figure: Soft Start



PCS (Primary Current Simulation)

A voltage proportional to the current of the power transistor is generated at Pin PCS by the RC-combination R2, C2. The voltage at Pin PCS is forced to 1.5V when the power transistor is switched off and during its switch on time C2 is charged by R2 from the rectified mains. The relation of V_{PCS} and

the current in the power transistor (Iprimary) is:

$$VPCS = 1,5V + \frac{Lprimary \times Iprimary}{R2 \times C2}$$

Lprimary: Primary inductance of the transformer

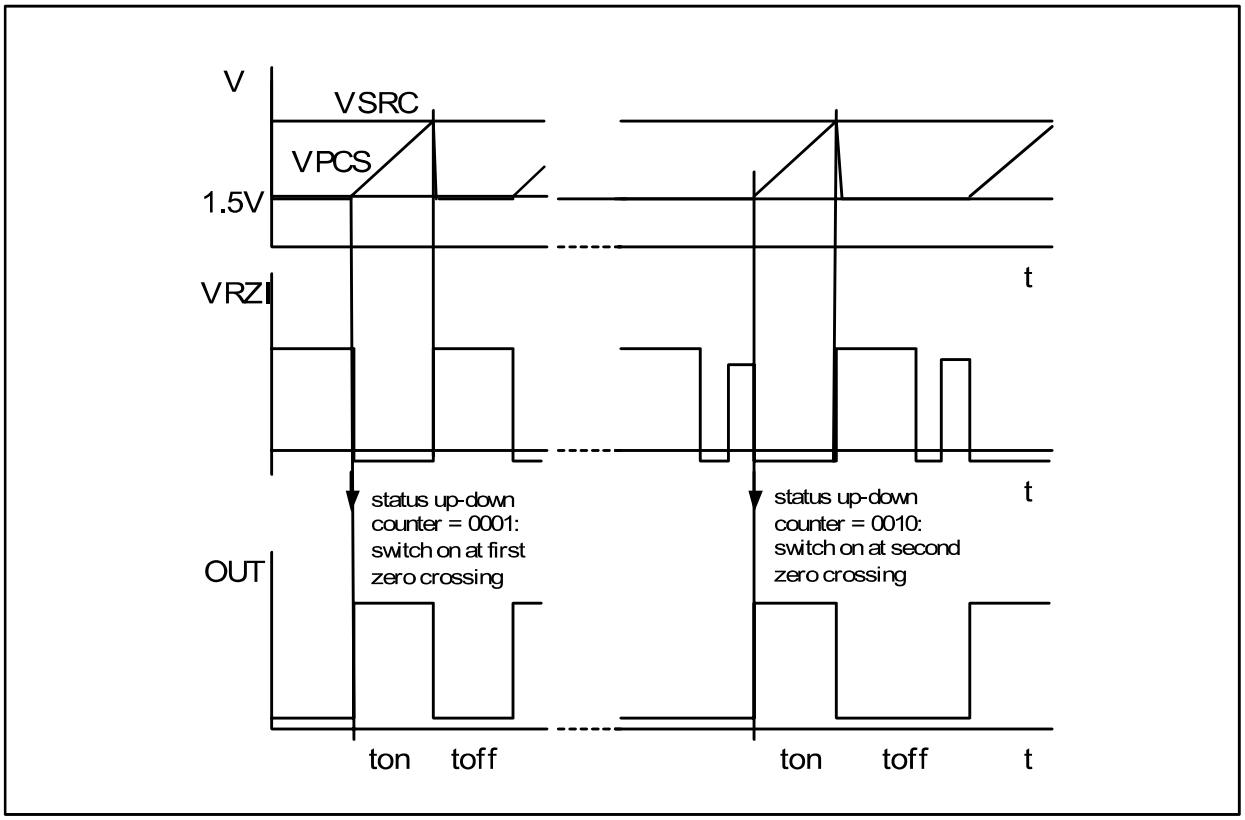
The advantage of primary current simulation is the elimination of the leading edge spike, which is generated when the power transistor is switched on.

RZI (zero crossing input and primary regulation)

Zero current counter

Every time when the falling voltage ramp of V_{RZI} crosses the 25 mV threshold a pulse is sent to the zero-current-counter and increases the counter by one. If zero-current-counter and up-down-counter are equal the gate drive OUT is switched to high. Up-down counter is influenced via SRC voltage as described below. If V_{RZI} is greater than 25 mV gate drive OUT is always switched low.

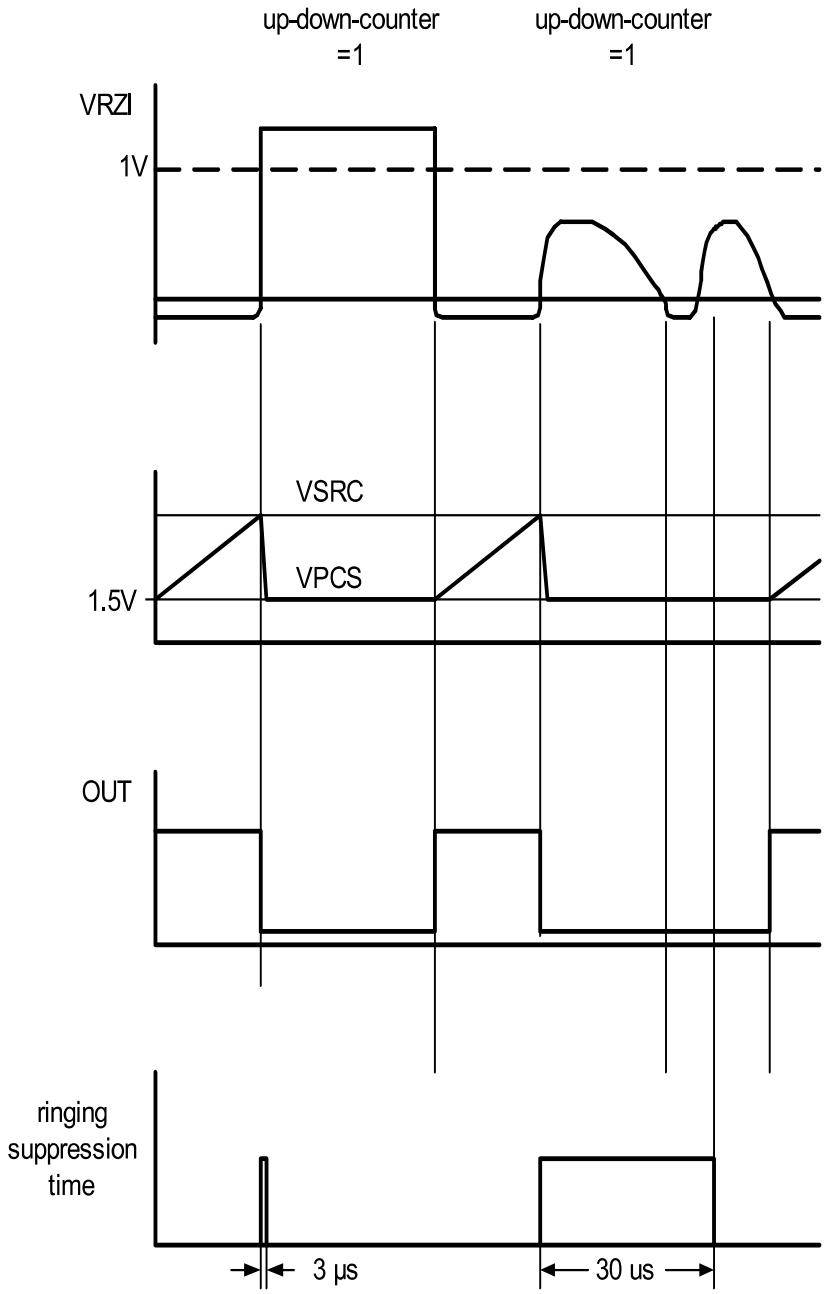
Figure: Zero crossing switching behaviour



Ringing suppression

When V_{PCS} reaches the feedback voltage V_{SRC} the gate drive OUT is set to low and the ringing suppression timer is started. This timer ensures that the gate drive cannot be switched on until this ringing suppression time is passed. Duration of ringing suppression time depends on the V_{RZI} voltage. Suppression time is 3 µsec if V_{RZI} > 1V and it is 30 µsec if V_{RZI} < 1V.

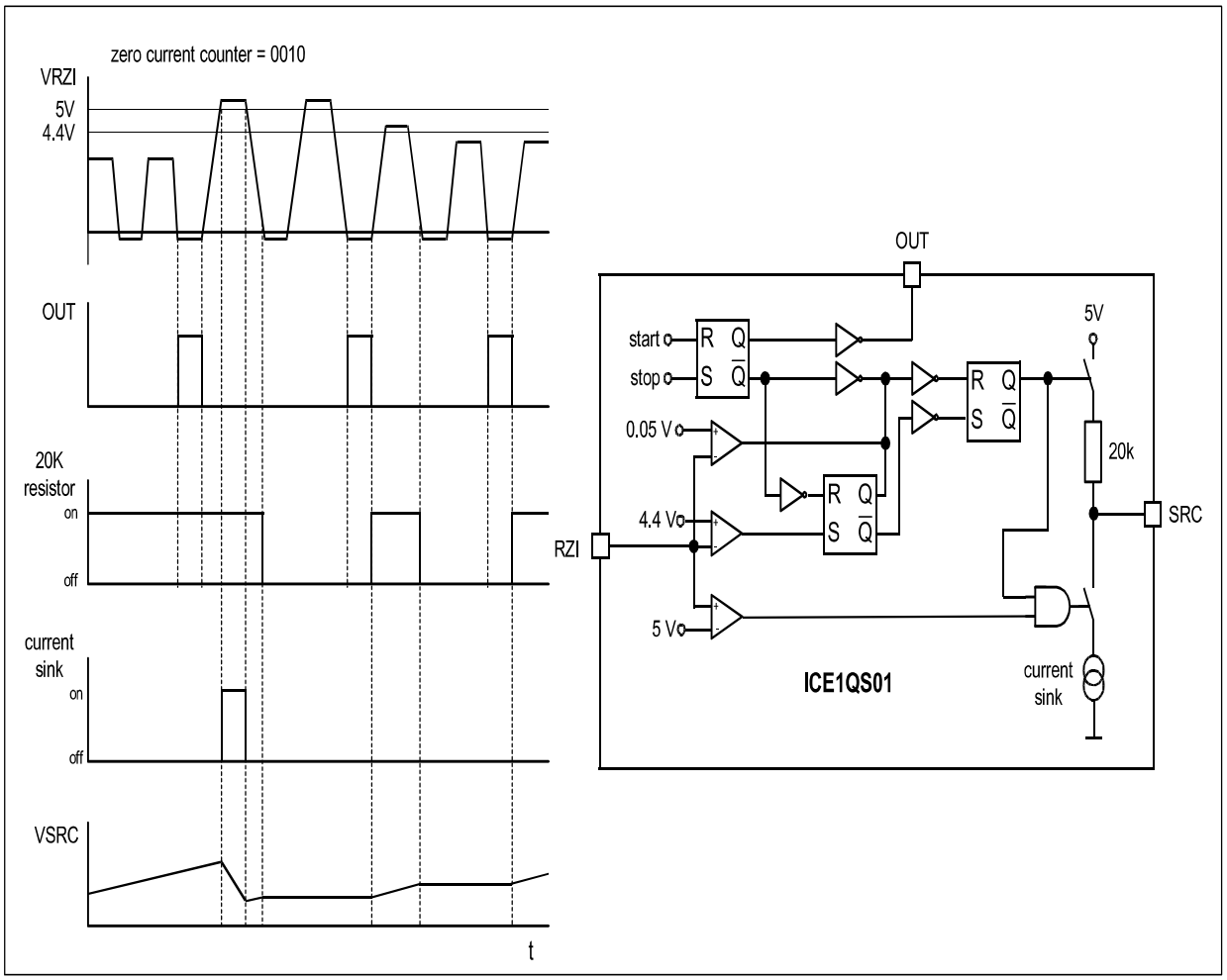
Figure: Ringing Suppression



Primary regulation

Primary regulation is achieved by activating the internal current sink. The current sink is connected between pin SRC and ground. If V_{RZI} exceeds the 5V threshold the current sink is switched on. It is switched off when V_{RZI} falls below 5V. The current sink discharges the C_{SRC} capacitor. C_{SRC} is charged via the internal 20k resistor. If V_{RZI} exceeds the 4.4V threshold a flip-flop is set and the resistor is switched off when V_{RZI} falls below 50 mV. The resistor is switched on again with the falling slope of gate drive OUT.

Diagram Primary Regulation



SRC (Regulation and soft start capacitor)

The feedback capacitor is connected to pin SRC. The feedback voltage V_{SRC} has two main functions.

Function I (MOS FET on time): V_{SRC} provides the switch off reference voltage. If V_{PCS} (which contains the primary current information) exceeds the V_{SRC} voltage the external MOS transistor is switched off.

Function II (MOS FET off time for frequency reduction): At low load the frequency is reduced by ignoring zero crossing signals after the transformer demagnetization. V_{SRC} determines the action of the 4-bit up-down-counter which contains the number of zero crossings to be ignored. The content of the up-down-counter is compared with the number of zero-current crossings of $V_{RZI.}$ If the number of zero-current crossings in each period after the transformer demagnetization is equal to the up-down-counter content the MOS is switched on. At low load conditions when V_{SRC} is below 3.5V the counter is increased by one every 50 msec. The result is that the MOS transistor off-time increases and duty cycle decreases. At high load conditions when V_{SRC} is higher than 4.4V the counter content is reduced by one every 50msec. So MOS transistor off-time will be reduced. With this off-time regulation switching jitter can be eliminated.

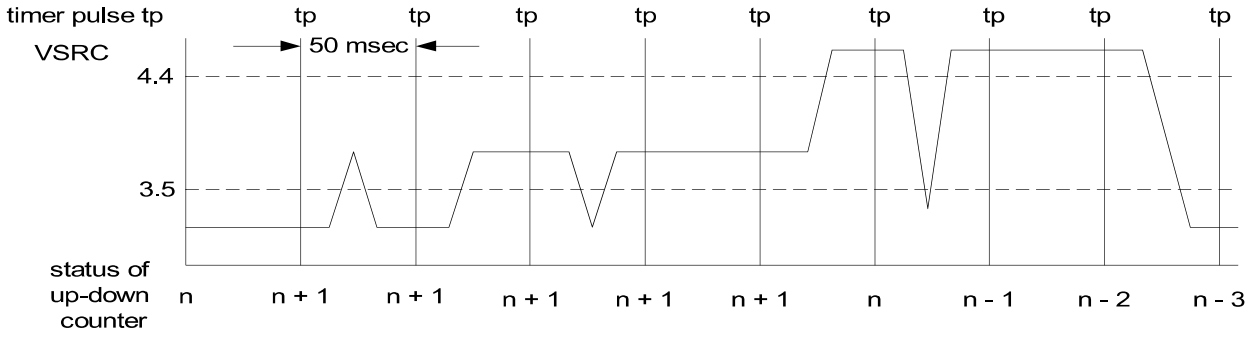
The up-down-counter is immediately set to 0001 if a load jump occurs and V_{SRC} exceeds 4.8 V. This ensures that full power can be provided instantaneously.

The following table shows the SRC voltage range and the corresponding up-down counter action.

SRC voltage range	up-down-counter action
1: VSRC< 3.5V	count forward
2: 3.5<VSRC<4.4	stop count
3: VSRC>4.4	count backward
4: VSRC> 4.8	set up-down-counter to1

The information provided by V_{SRC} is stored in two independent flip flops. An internal timer creates a trigger pulse with a period of 50 msec. Every time the pulse occures the up-down counter checks the status flip flops and acts depending on the flip flop information. After this pulse the flip flops are reset. So change of voltage range is noticed by the logic only once during the 50 ms period. In the diagram below the behaviour of the up-down counter is depicted in more detail.

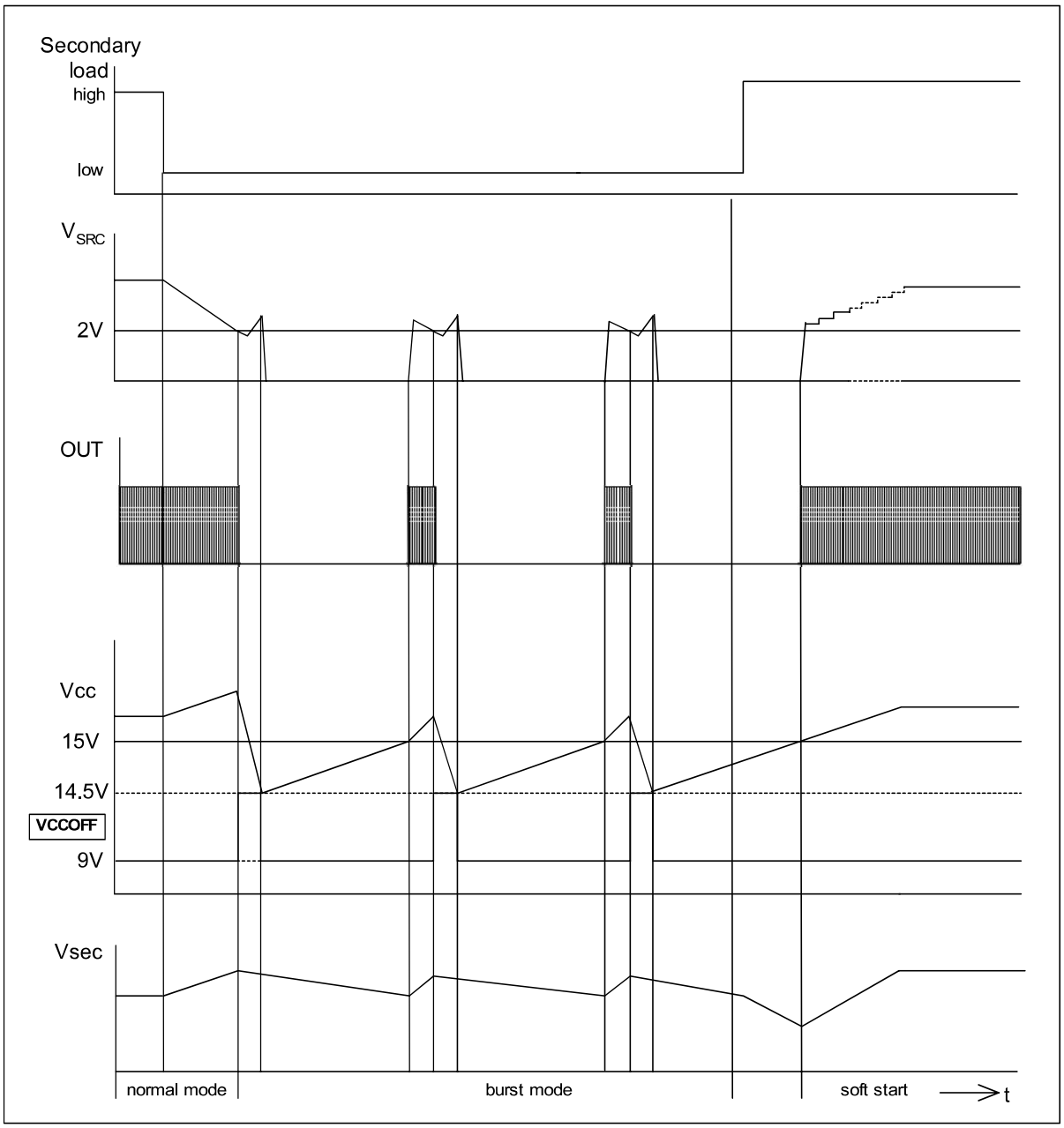
Diagram 1



Burst mode

12 µsec after beginning of softstart the burst mode comparator is activated. If V_{SRC} falls below 2V after activating the comparator the gate drive OUT is switched to low and the V_{CCoff} threshold is changed to 14.5 V. V_{CC} decreases because gate drive is held low. If V_{CC} reaches the V_{CCoff} threshold the IC is going into start-up mode. At V_{CCon} threshold the IC is switched on again starting with soft start modus. V_{CCoff} threshold is set to the normal 9V.

Figure: Burst mode



Restart timer

If voltage V_{RZI} is lower than 50 mV and gate drive OUT is low an internally created restart pulse will switch gate drive OUT high every 50 µs and the minimum switching frequency is about 20 kHz.

Restart pulse is inhibited if V_{RZI} is higher than 50 mV. So the MOS transistor cannot be switched on until the transformer is discharged.

VCC overvoltage protection

If V_{CC} exceeds the V_{CCD} threshold a latch is set and the gate is disabled. Reset of latch occurs when V_{CC} is falling below V_{CCon}- V_{CCBHY}.

Overvoltage fault comparator (OFC)

With an external sense resistor connected to pin OFC primary current can be sensed directly. If the sensed current exceeds the internal V_{OFC} threshold a latch is set and gate is disabled. Reset of latch occurs when V_{CC} is falling below V_{CCon}- V_{CCBHY}.

Notice: If this comparator is not used pin OFC has to be connected to ground.

Mains undervoltage

Power supplies must be shut down when mains voltage is below a certain limit to avoid too long on-time of MOS-FET switch, which would lead to a switching frequency in audible spheres. Mains undervoltage is sensed during the off-time of the MOS-FET switch. If the current flowing into pin PCS is smaller than 100 uA, then the output is latched and cannot be switched to high state.

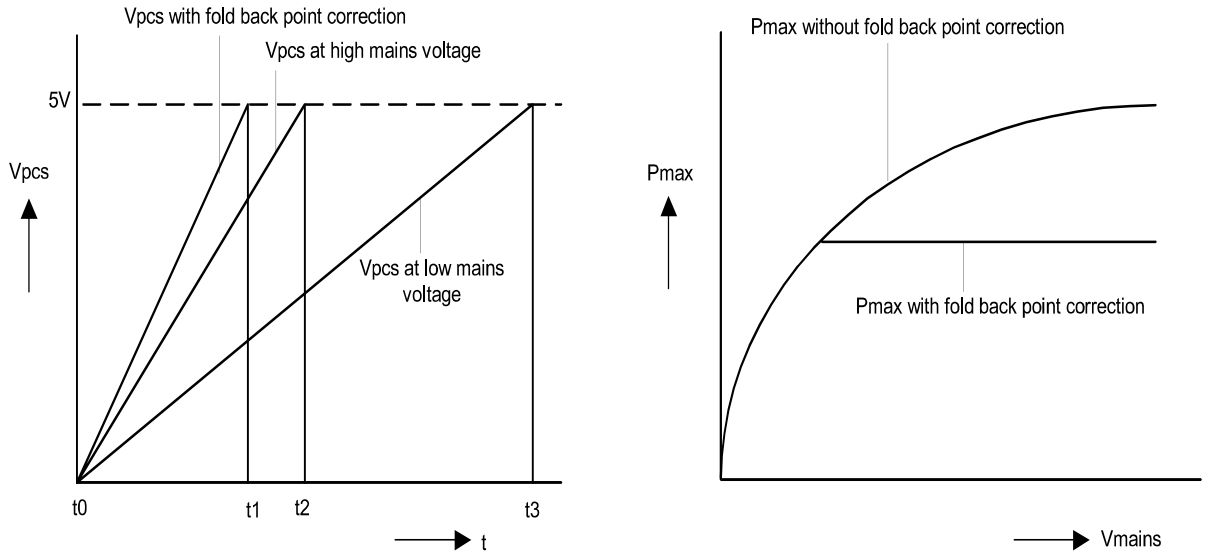
Fold back point correction

With increasing mains voltage the switch on time becomes shorter and so the frequency becomes higher. With higher frequency also the maximal possible output power becomes higher. With higher power the danger in case of failure increases.

To avoid this, the foldback point correction circuit senses main voltage to reduce the on-time of the switch. Mains voltage is sensed at the supply coil of V_{CC} voltage via a resistor connected to pin RZI. During on-time of the MOS-FET switch current is pulled out from pin RZI. When this current is higher than 500 µA, one fifth of the current higher than this threshold is driven into pin PCS to increase the voltage slope charging the capacitor connected to this pin.

$$IPCSFO = \frac{IRZI - 0,5mA}{5}, (IRZI > 500uA)$$

Figure: Fold back point correction



Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit	Remark
Charge Current into Pin2	I_{PCS}		500	uA	During start up
Voltage at Pin 2	V_{PCS}	-0.3	21	V	
Current into Pin 3	I_{RZI} I_{RZI}	 -10	10	mA mA	$V_{RZI}>V_{RZICH}$ $V_{RZI}<V_{RZICL}$
Voltage at Pin 4	V_{SRC}	-0.3	V_{SRCCL}	V	I_{SRC}=100 µA
Voltage at Pin 5	V_{OFC}	-0.3	6	V	
Current into Pin 7	I_{OUT}	-500	500	mA	t<1ms
Voltage at Pin 8	V_{CC}	-0.3	21	V	
ESD Protection			4000	V	MIL STD 883C method 3015.6, 100pF,1500Ω
Storage Temperature	T_{stg}	-50	150	°C	
Operating Junction Temperature	T_J	-25	150	°C	
Thermal Resistance Junction-Ambient	R_{thJA}		100	K/W	P-DIP-8

Characteristics (Unless otherwise stated, -25°C<Tj <150 °C, VCC = 16V)

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Start-Up circuit						
Start-up supply current	I_{CCL}		60	100	µA	$V_{CC}=V_{CCon}$-0.5V
Operating supply current	I_{CCH}		10		mA	Output low
V_{CC} Turn-On threshold	$V_{CC\ ON}$	14.1	15	15.5	V	
V_{CC} Turn-Off threshold	$V_{CC\ OFF}$	8.5	9	9.5	V	
V_{CC} Hysteresis	V_{CCHY}		6		V	
V_{CC} Burst Hysteresis	V_{CCBHY}		0.5		V	
V_{CC} Overvoltage	V_{CCD}		20		V	t > 1.5µsec
SRC soft start mode						
Start Voltage	V_{SRC1}		2.5		V	$I_{optocoupler}$=0 µA
Digital voltage step	V_{SRCST}		360		mV	$I_{optocoupler}$=0 µA
Step pulse rate	t_{SRCSTR}		3		ms	
Soft start time	t_{ST}		24		ms	
Current source rise time	t_{STRT}		9		µs	V_{SRC}=0.2V to 2.0V C_{SRC}=10nF
Current source on time	t_{STOT}		12		µs	
SRC normal mode						
Source resistor	R_{SRC}		20		kOhm	
Clamping threshold voltage	V_{SRCCL}		5		V	$V_{PCS}=V_{SRC}$, OUT switches to Low, I_{SRC}=100µA
Threshold upward count	V_{SRCSU}		3.5		V	
Threshold downward count	V_{SRCD}		4.4		V	
Reset counter to one	V_{SRCR}		4.8		V	
Counter time [1)]	t_{COUNT}		50		msec	
Sink current prim reg mode	I_{SRCS}		500		µA	V_{RZI} > 5V
Burst mode latch threshold voltage	V_{SRCB}		2.0		V	V_{SRC} <V_{SRCB}: OUT=Low

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
RZI (regulation and zero crossing input)						
Zero crossing threshold voltage	V_{RZIT}		50		mV	V_{RZI}<V_{RZIT}: Out=High
Time delay switch on	t_{don}		500		nsec	
Biascurrent	I_{RZIB}		25		µA	V_{RZI}=5V
Clamping voltage low state	V_{RZICL}		-0.2		V	I_{RZI} = -1mA
Clamping voltage high state	V_{RZICH}		5.7		V	I_{RZI}= 5mA
Primary regulation threshold discharge current	V_{RZIDC}		5		V	
Primary regulation threshold charge current	V_{RZICC}		4.4		V	
Ringing suppression threshold voltage	V_{RZIT}		1		V	
Ringing suppression time	t_{RZIP} t_{RZIP}		2.5 25		µsec µsec	V_{RZI} > V_{RZIT} V_{RZI} < V_{RZIT}
Foldback point correction current threshold	I_{PCSF}		500		µA	
PCS (primary current simulation)						
Gate enable threshold voltage	V_{PCSE}		1.0		V	V_{PCS}<V_{PCSE}: Out=Low
Basic voltage	V_{PCSB}		1.5		V	gate low
Shut down delay	t_{SRC}		100		nsec	
Mains undervoltage lockout current	I_{PCS}		100		µA	
Voltage drop startup diode	V_{PCSD}		0.7		V	I_{PCS}=300µA
Discharge current	I_{PCSD}		4		mA	V_{PCS}=3V
OFC (overcurrent fault comparator)						
Bias Current	I_{OFCB}	-1			µA	
Gate drive disabled threshold voltage	V_{OFC}		1.0	1.05	V	
Shut Down Delay	t_{OFC}		100		ns	

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Restart Timer						
Restart time	t_{RES}			55	µs	V_{RZI}<25mV
Gate Drive						
Output voltage low			1		V	
Output voltage high			11		V	
Output voltage active shut down			1		V	V_{CC}=7V I_{OUT}=20mA
Rise time			70		ns	C_{OUT}=1nF
Fall time			55		ns	C_{OUT}=1nF

Figure: Circuit Diagram for Standard Application

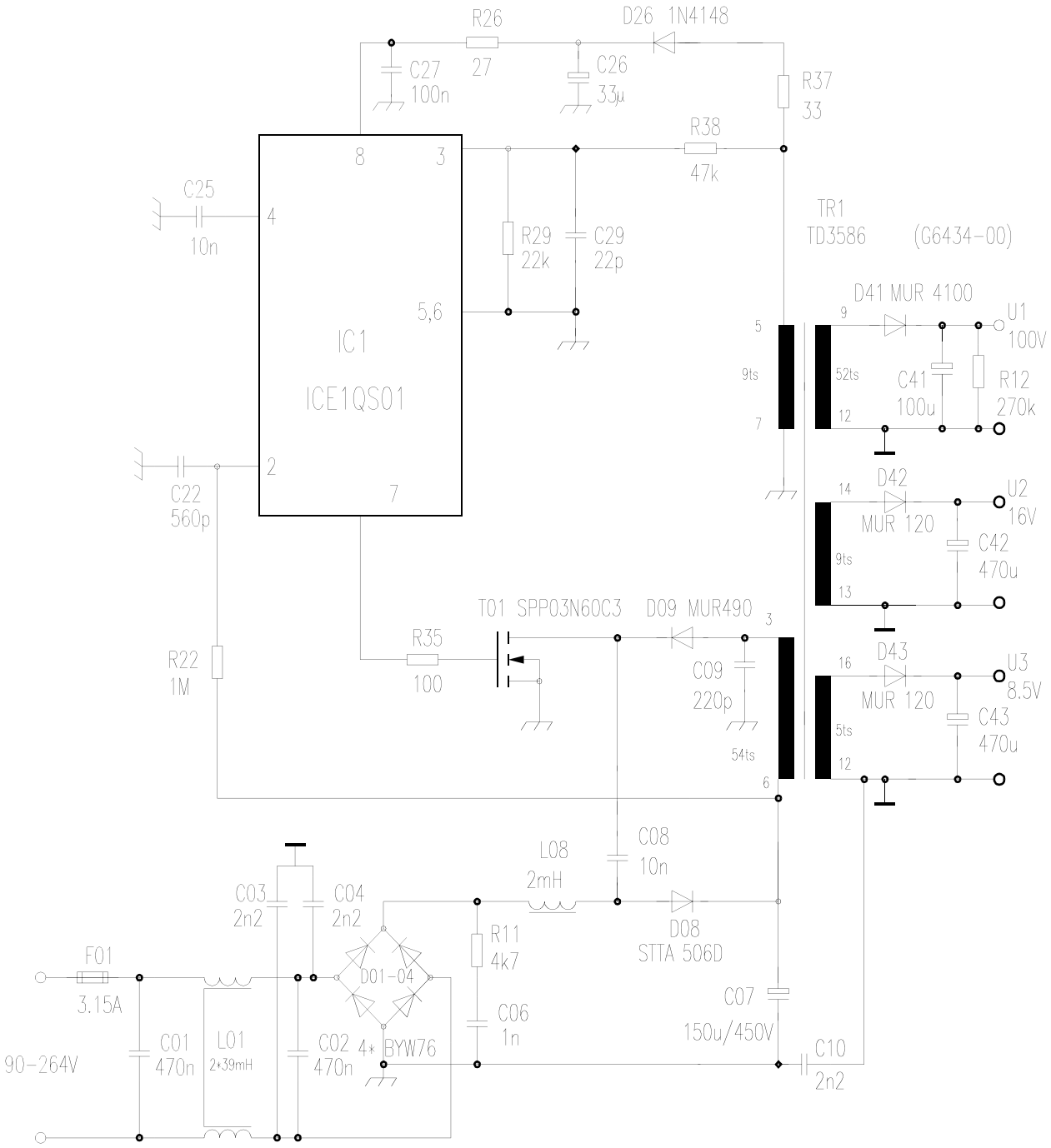
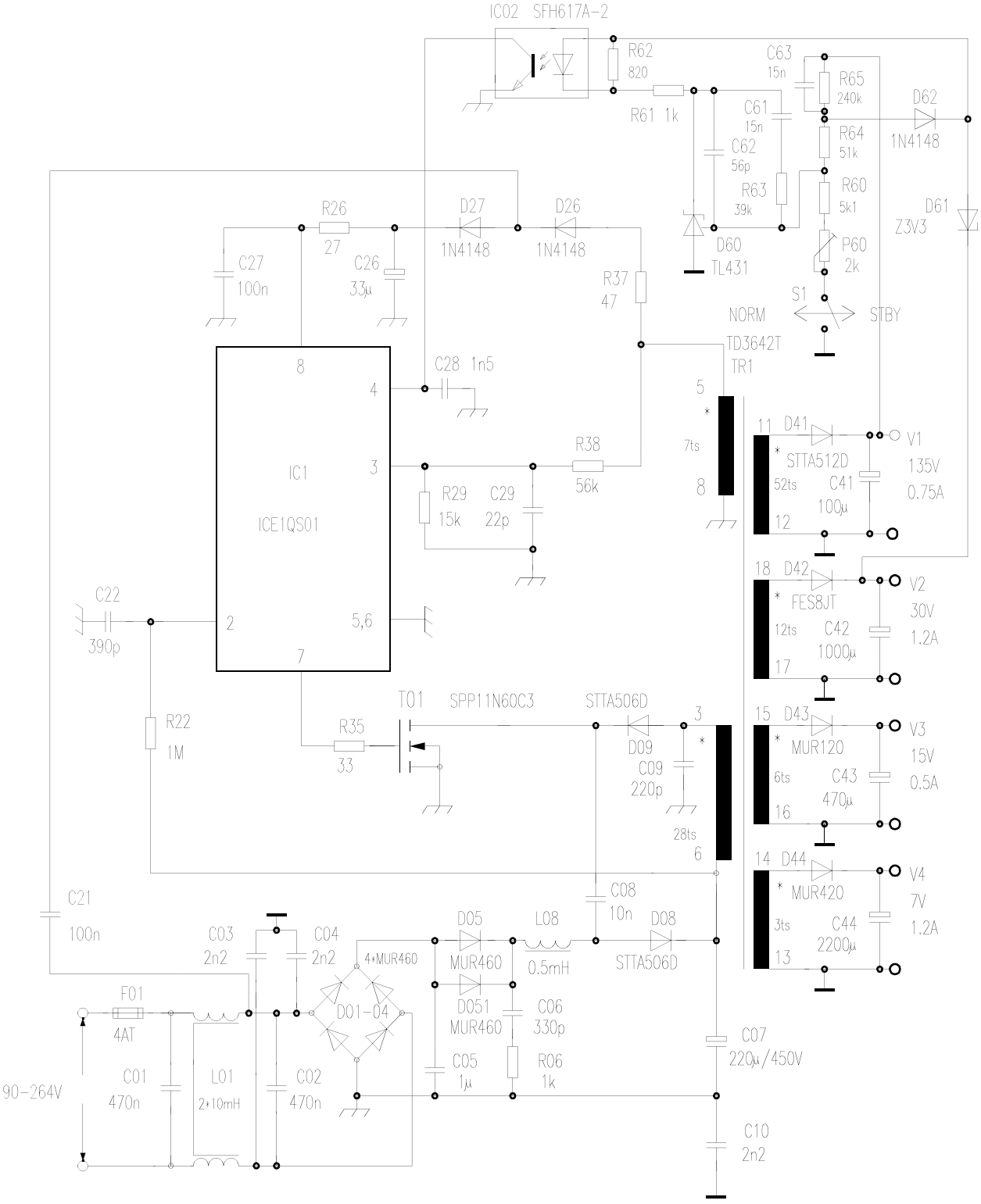
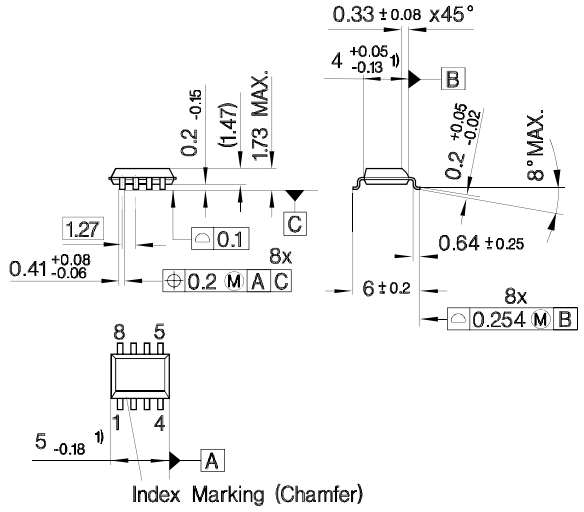


Figure: Circuit Diagram for Application with PFC and Low Voltage Standby Mode



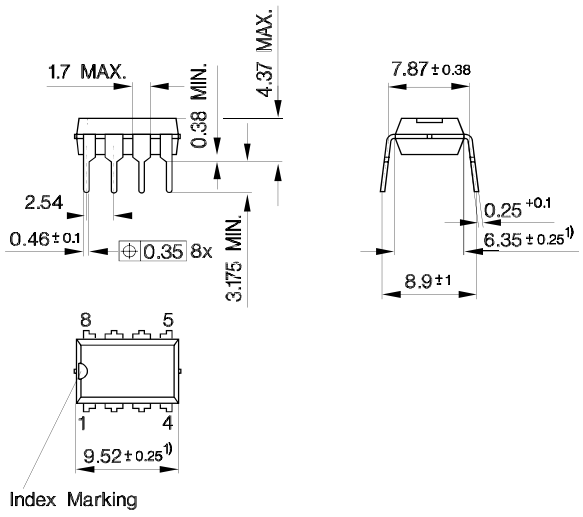
Plastic Package, P-DSO-8-3
(Plastic Dual Small Outline Package)



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GPS05121

Plastic Package, P-DIP-8-4
(Plastic Dual In-line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05025

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

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