Ordering number: EN 4342A

Thick Film Hybrid IC

# STK401-030

## 2ch AF Power Amplifier (Split Power Supply) (20W +20W min, THD = 0.4%)

## Overview

The STK401-030 is a thick-film audio power amplifier IC belonging to a series in which all devices are pin compatible. This allows a single PCB design to be used to construct amplifiers of various output capacity simply by changing hybrid ICs. Also, this series is part of a new, larger series that comprises mutually similar devices with the same pin compatibility. This makes possible the development of a 2-channel amplifier from a 3-channel amplifier using the same PCB. In addition, this new series features 6/3Ω drive in order to support the low impedance of modern speakers.

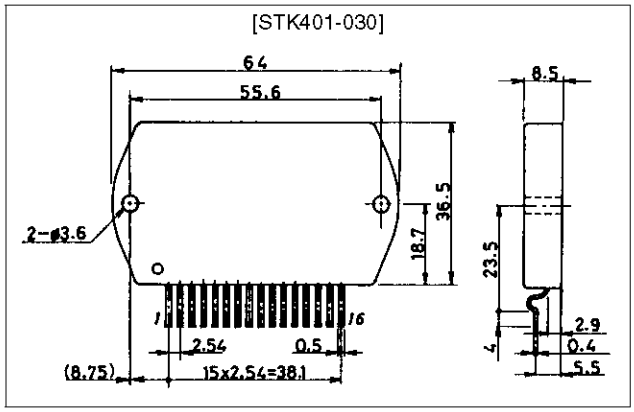
## Features

- Pin compatible
  STK400-000 series (3-channel/single package)
  ↓
  STK401-000 series (2-channel/single package)
- Output load impedance $R_L$ = 6/3Ω supported
- New pin configuration
  Pin configuration has been grouped into individual blocks of inputs, outputs and supply lines, minimizing the adverse effects of pattern layout on operating characteristics.
- Few external components
  In comparison with existing series, external bootstrap resistors and capacitors can be eliminated.

## Package Dimensions

unit: mm

**4134**



# Specifications

## Maximum Ratings at Ta = 25°C

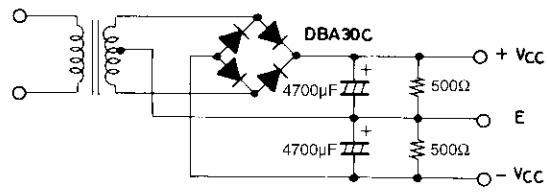
| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$ max | | ±34 | V |
| Thermal resistance | θj-c | Per power transistor | 2.1 | °C/W |
| Junction temperature | Tj | | 150 | °C |
| Operating substrate temperature | Tc | | 125 | °C |
| Storage temperature | Tstg | | –30 to +125 | °C |
| Available time for load short-circuit | $t_s$ | $V_{CC}$ = ±23V, $R_L$ = 6Ω, f = 50Hz, $P_O$ = 20W | 1 | s |

## Operating Characteristics at Ta = 25°C, $R_L$ = 6Ω (noninductive load), Rg = 600Ω, VG = 40dB

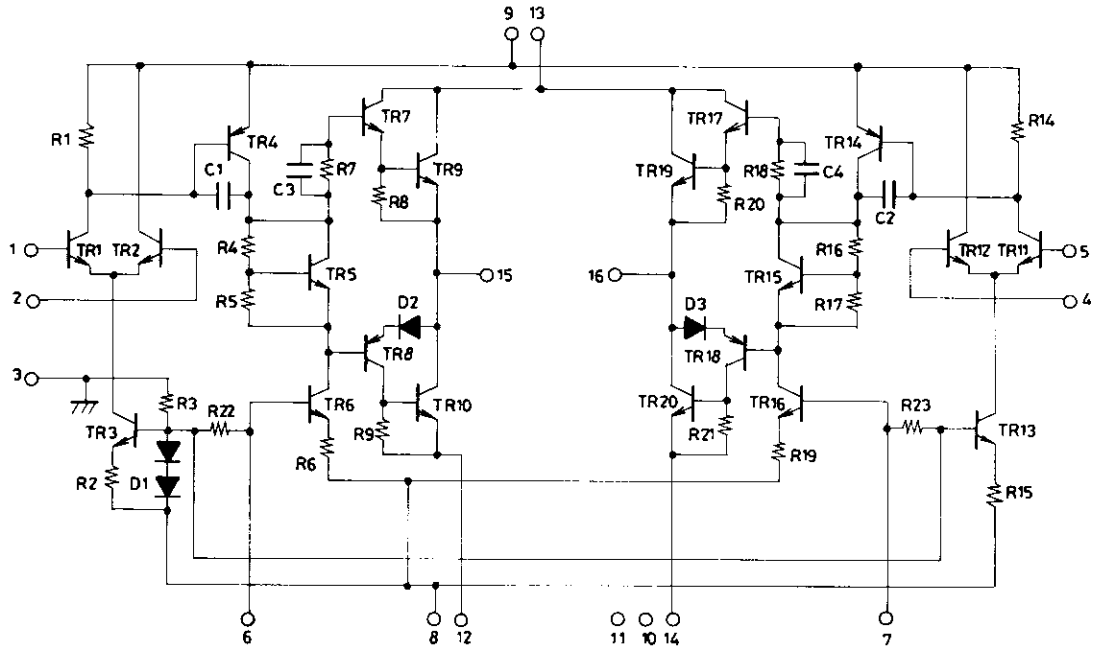
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Quiescent current | $I_{CCO}$ | $V_{CC}$ = ±28V | 20 | 60 | 100 | mA |
| Output power | $P_O$(1) | $V_{CC}$ = ±23V, f = 20Hz to 20kHz, THD = 0.4% | 20 | 25 | – | W |
| | $P_O$(2) | $V_{CC}$ = ±19V, f = 1kHz, THD = 1.0%, $R_L$ = 3Ω | 20 | 25 | – | W |
| Total harmonic distortion | THD(1) | $V_{CC}$ = ±23V, f = 20Hz to 20kHz, $P_O$ = 1.0W | – | – | 0.4 | % |
| | THD(2) | $V_{CC}$ = ±23V, f = 1kHz, $P_O$ = 5.0W | – | 0.02 | – | % |
| Frequency response | $f_L$, $f_H$ | $V_{CC}$ = ±23V, $P_O$ = 1.0W, $^{+0}_{-3}$dB | – | 20 to 50k | – | Hz |
| Input impedance | $r_i$ | $V_{CC}$ = ±23V, f = 1kHz, $P_O$ = 1.0W | – | 55 | – | kΩ |
| Output noise voltage | $V_{NO}$ | $V_{CC}$ = ±28V, Rg = 10kΩ | – | – | 1.2 | mVrms |
| Neutral voltage | $V_N$ | $V_{CC}$ = ±28V | –70 | 0 | +70 | mV |

Notes.
All tests are measured using a constant-voltage supply unless otherwise specified.
Available time for load short-circuit and output noise voltage are measured using the transformer supply specified below.
The output noise voltage is the peak value of an average-reading meter with an rms value scale (VTVM). A regulated AC supply (50Hz) should be used to eliminate the effects of AC primary line flicker noise.

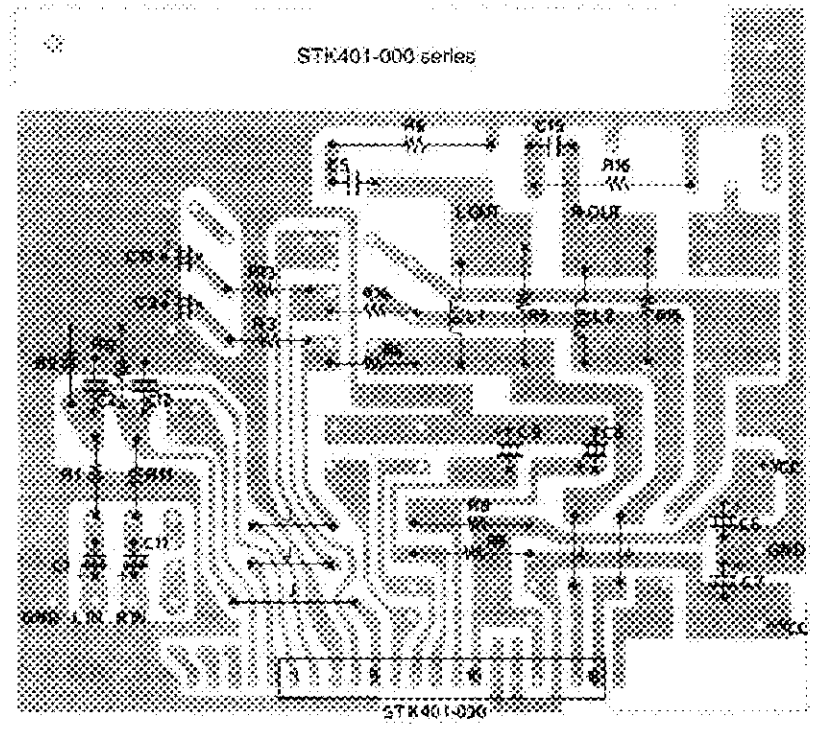
## Specified Transformer Supply (RP-25 or Equivalent)



## Equivalent Circuit

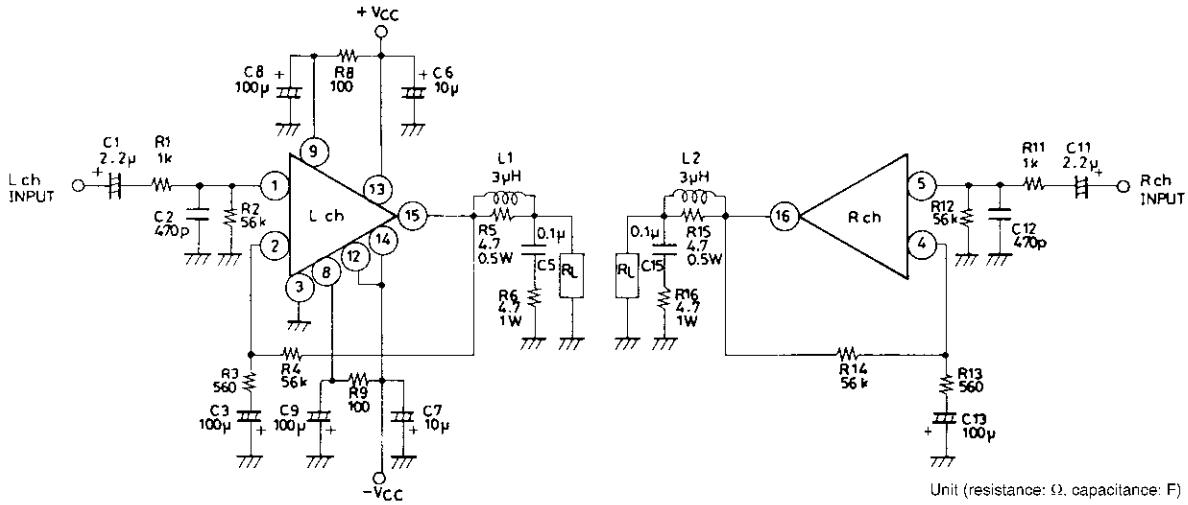



## Sample PCB Layout for 2-Channel or 3-Channel Amplifiers




Copper (Cu) foil surface
Pin 6 of STK400-000 series devices corresponds to pin 1 of STK401-000 series devices.

## Sample Application Circuit




Unit (resistance: Ω, capacitance: F)

## External Component Description

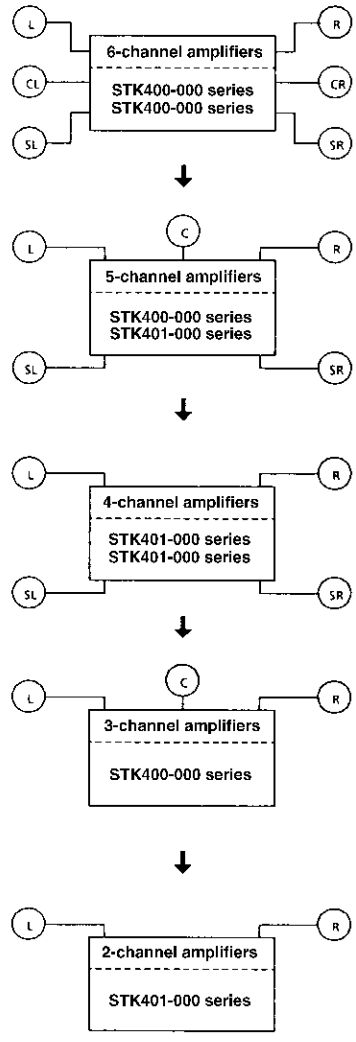
| | |
|---|---|
| C1, C11 | Input coupling capacitors.<br>For DC blocking. Since capacitor reactance becomes larger at lower frequencies, the output noise can be adversely affected by signal source resistance-dependent 1/f noise. In this case, a lower reactance value should be chosen. In order to remove pop noise at power-on, larger values of capacitance should be chosen for C1 and C11, which determine the input time constant, and smaller values for C3 and C13 in the NF circuit. |
| C2, C12 | Input filter capacitors.<br>These, together with R1 and R11, form filters to reduce high-frequency noise. |
| C3, C13 | NF capacitors.<br>These determine the low-side cut-off frequency.<br>$f_L = \frac{1}{2\pi \times C3(C13) \times R3(R13)}$<br>Large values should be chosen for C3 and C13 to maintain voltage gain at low frequencies. However, because this would tend to increase the shock noise at power-on, values larger than absolutely necessary should be avoided. |
| C5, C15 | Oscillation prevention capacitors.<br>Mylar capacitors are recommended for their excellent thermal and frequency characteristics. |
| C6, C7 | Oscillation prevention capacitors.<br>These should be inserted as close as possible to the IC supply pins to reduce supply impedance and hence provide stable IC operation. Electrolytic capacitors are recommended. |
| C8, C9 | Decoupling capacitors.<br>These, together with R8 and R9, form time constant circuits that remove shock noise and ripple voltage from the supply, preventing any noise being coupled to the inputs. |
| R1, R11 | Input filter resistors. |
| R2, R12 | Input bias resistors.<br>These are used to bias the input pins at zero potential. The input impedance is largely determined by this resistance. |
| R3, R13<br>R4, R14 | Voltage-gain VG setting resistors.<br>VG = 40dB is recommended using R3, R13 = 560Ω, and R4, R14 = 56kΩ. Gain adjustments are best made using R3 and R13. If gain adjustments are made using R4 and R14, then set R2, R12 = R4, R14 to maintain $V_N$ balance stability. |
| R5, R15 | Oscillation prevention resistors. |
| R6, R16 | Oscillation prevention resistors.<br>The power dissipated in these resistors is dependent on the frequency, as given below.<br>$P_{R6(R16)} = \left(\frac{V_{CC}\ max/\sqrt{2}}{1/2\pi f \times C5(C15) + R6(R16)}\right)^2 \times R6(R16)$<br>where f is the output signal frequency upper limit. |
| R8, R9 | Ripple filter resistors.<br>$P_O$ max, ripple rejection and supply power-on shock noise are all affected by this resistance. These resistors should be chosen taking into consideration both the function they perform as predriver transistor limiting resistors during load short circuits and the peak current that flows through them when charging C8 and C9. |
| L1, L2 | Oscillation prevention coils.<br>These correct the phase difference caused by capacitive loads and increase stability against oscillation. |

## Series Configuration

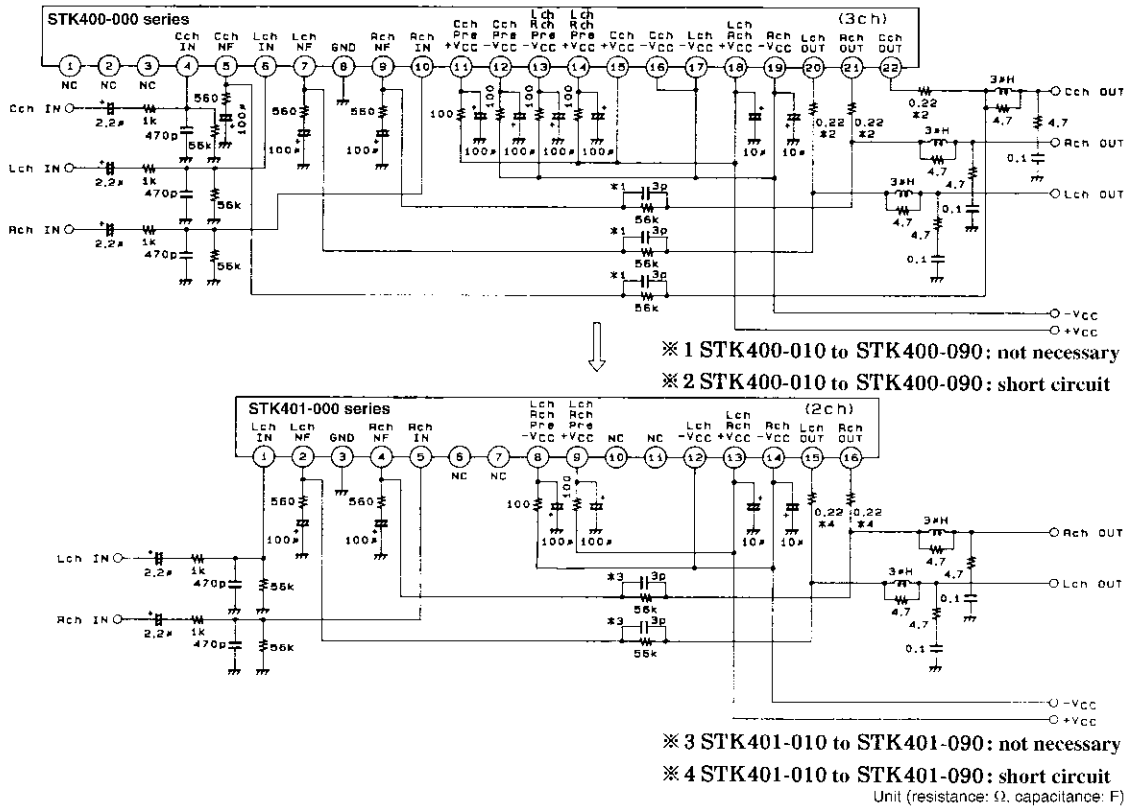
| 3-channel amplifier type Nos. | Rated output | 2-channel amplifier type Nos. | Rated output | THD [%] f = 20Hz to 20kHz | Supply voltage [V][1] | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{CC}$ max1 | $V_{CC}$ max2 | $V_{CC}$1 | $V_{CC}$2 |
| STK400-010 | 10W × 3 | STK401-010 | 10W × 2 | 0.4 | – | ±26 | ±17.5 | ±14 |
| STK400-020 | 15W × 3 | STK401-020 | 15W × 2 | | – | ±29 | ±20 | ±16 |
| STK400-030 | 20W × 3 | STK401-030 | 20W × 2 | | – | ±34 | ±23 | ±19 |
| STK400-040 | 25W × 3 | STK401-040 | 25W × 2 | | – | ±36 | ±25 | ±21 |
| STK400-050 | 30W × 3 | STK401-050 | 30W × 2 | | – | ±39 | ±26 | ±22 |
| STK400-060 | 35W × 3 | STK401-060 | 35W × 2 | | – | ±41 | ±28 | ±23 |
| STK400-070 | 40W × 3 | STK401-070 | 40W × 2 | | – | ±44 | ±30 | ±24 |
| STK400-080 | 45W × 3 | STK401-080 | 45W × 2 | | – | ±45 | ±31 | ±25 |
| STK400-090 | 50W × 3 | STK401-090 | 50W × 2 | | – | ±47 | ±32 | ±26 |
| STK400-100 | 60W × 3 | STK401-100 | 60W × 2 | | – | ±51 | ±35 | ±27 |
| STK400-110 | 70W × 3 | STK401-110 | 70W × 2 | | ±56.0 | – | ±38 | – |
| – | – | STK401-120 | 80W × 2 | | ±61.0 | – | ±42 | – |
| – | – | STK401-130 | 100W × 2 | | ±65.0 | – | ±45 | – |
| – | – | STK401-140 | 120W × 2 | | ±74.0 | – | ±51 | – |

1. $V_{CC}$ max1 ($R_L$ = 6Ω), $V_{CC}$ max2 ($R_L$ = 3 to 6Ω), $V_{CC}$1 ($R_L$ = 6Ω), $V_{CC}$2 ($R_L$ = 3Ω)

## Sample Designs using a Common PCB



## External Circuit Diagram




## Heatsink Design Considerations

The heatsink thermal resistance, θc-a, required to dissipate the STK401-030 device total power dissipation, Pd, is determined as follows:

Condition 1: IC substrate temperature not to exceed 125°C.

$$Pd \times \theta c\text{-}a + Ta < 125°C \quad \ldots\ldots (1)$$

where Ta is the guaranteed maximum ambient temperature.

Condition 2: Power transistor junction temperature, Tj, not to exceed 150°C.

$$Pd \times \theta c\text{-}a + Pd/N \times \theta j\text{-}c + Ta < 150°C \quad \ldots\ldots (2)$$

where N is the number of power transistors and θj-c is the power transistor thermal resistance per transistor. Note that the power dissipated per transistor is the total, Pd, divided evenly among the N power transistors.

Expressions (1) and (2) can be rewritten making θc-a the subject.

$$\theta c\text{-}a < (125 - Ta)/Pd \quad \ldots\ldots (1)'$$

$$\theta c\text{-}a < (150 - Ta)/Pd - \theta j\text{-}c/N \quad \ldots\ldots (2)'$$

The heatsink required must have a thermal resistance that simultaneously satisfies both expressions.

The heatsink thermal resistance can be determined from (1)′ and (2)′ once the following parameters have been defined.

- Supply voltage, $V_{CC}$
- Load resistance, $R_L$
- Guaranteed maximum ambient temperature, Ta

The total device power dissipation when STK401-030 $V_{CC} = \pm 23V$ and $R_L = 6\Omega$, for a continuous sine wave signal, is a maximum of 36.4W, as shown in Figure 1.

When estimating the power dissipation for an actual audio signal input, the rule of thumb is to select Pd corresponding to 1/10 $P_O$ max (within safe limits) for a continuous sine wave input. For example, from Figure 1,

$$Pd = 20.7W \text{ (for } 1/10\ P_O \text{ max} = 2W)$$

The STK401-030 has 4 power transistors, and the thermal resistance per transistor, θj-c, is 2.1°C/W. If the guaranteed maximum ambient temperature, Ta, is 50°C, then the required heatsink thermal resistance, θc-a, is:

From expression (1)′: $\theta c\text{-}a < (125 - 50)/20.7$
$< 3.62$

From expression (2)′: $\theta c\text{-}a < (150 - 50)/20.7 - 2.1/4$
$< 4.31$

Therefore, to satisfy both expressions, the required heatsink must have a thermal resistance less than 3.62°C/W.

Similarly, when STK401-030 $V_{CC}$ = ±19V and $R_L$ = 3Ω, from Figure 2:

Pd = 24.2W (for 1/10 $P_O$ max = 2W)

From expression (1)′: θc-a < (125 – 50)/24.2
< 3.10

From expression (2)′: θc-a < (150 – 50)/24.2 – 2.1/4
< 3.61

Therefore, to satisfy both expressions, the required heatsink must have a thermal resistance less than 3.10°C/W.

This heatsink design example is based on a constant-voltage supply, and should be verified within your specific set environment.

Figure 1. Pd — $P_O$

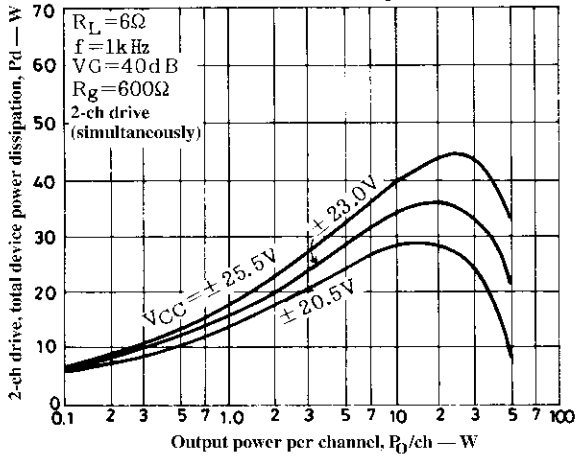
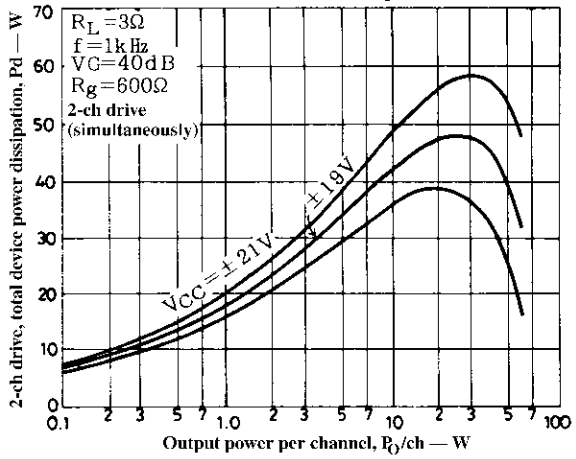
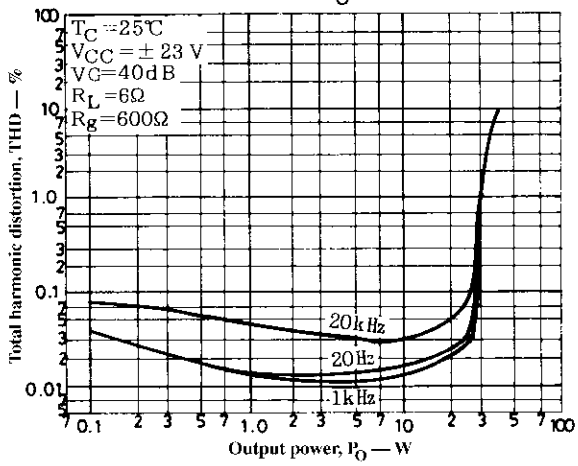


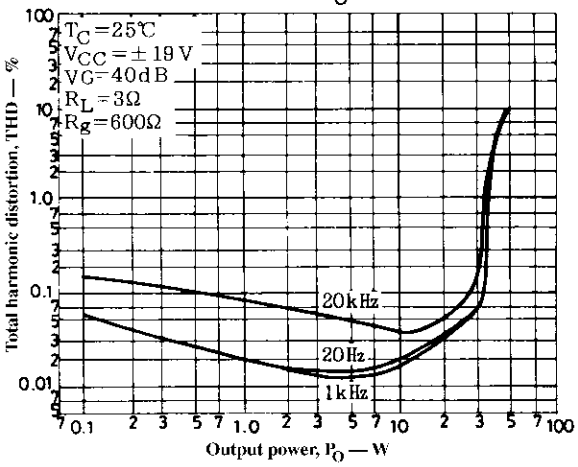

Figure 2. Pd — $P_O$



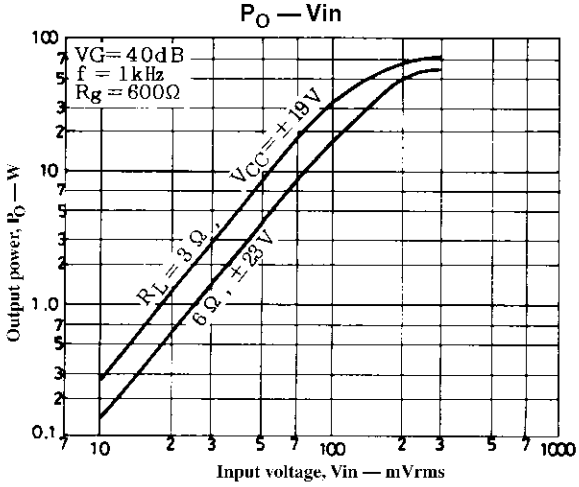

THD — $P_O$



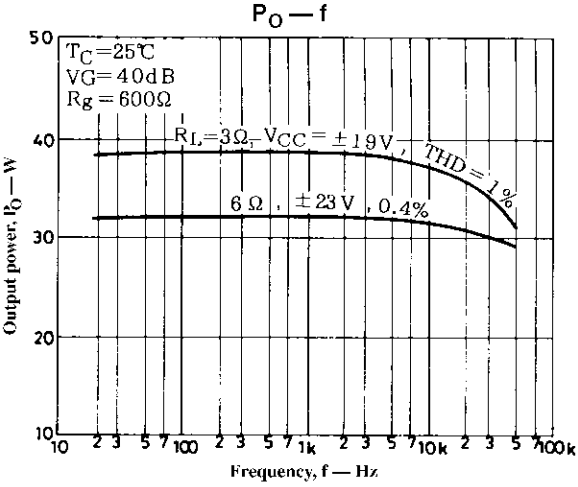

THD — $P_O$



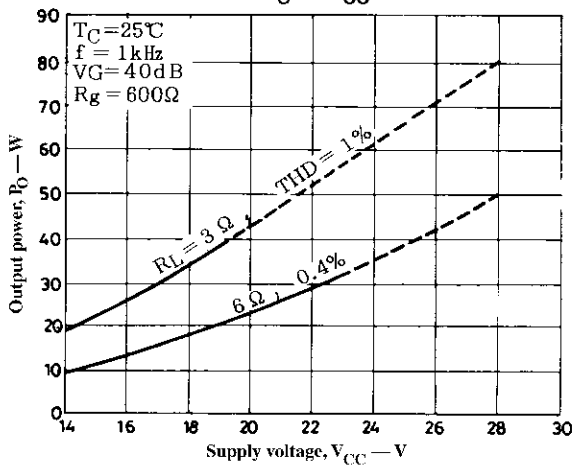

$P_O$ — Vin



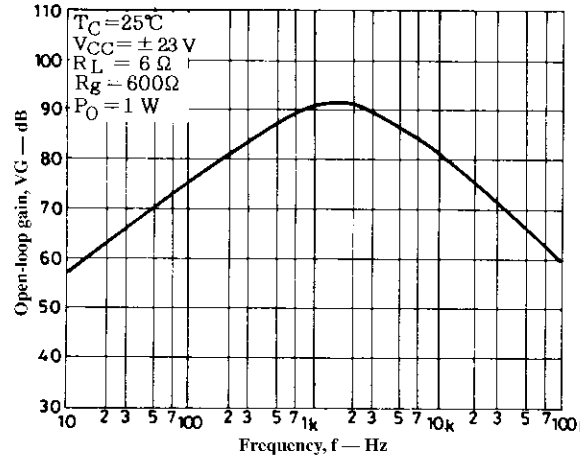

$P_O$ — f



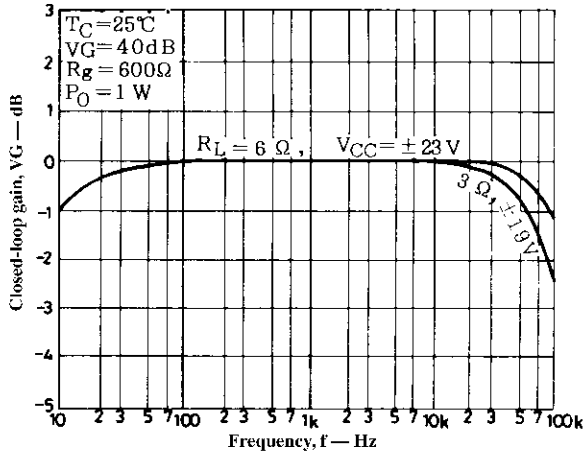
$P_O$ — $V_{CC}$



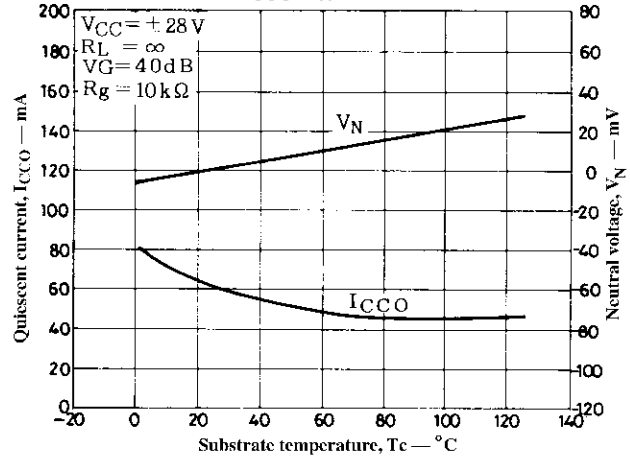

VG — f



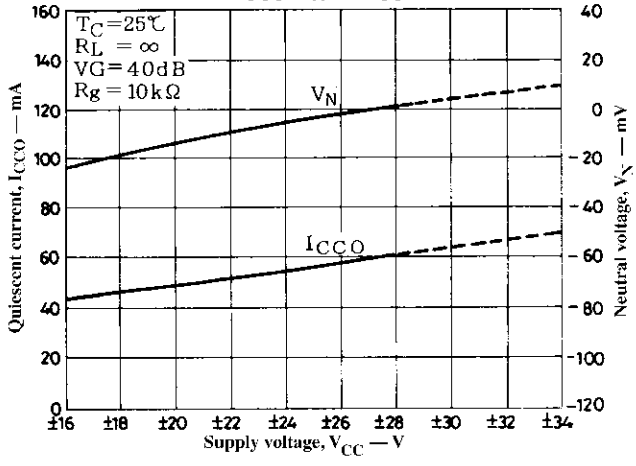

VG — f




$I_{CCO}$, $V_N$ — Tc




$I_{CCO}$, $V_N$ — $V_{CC}$





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