3.1A, 100V, 1.200 Ohm, P-Channel Power MOSFETs

These are advanced power MOSFETs designed, tested, and guaranteed to withstand a specific level of energy in the avalanche breakdown mode of operation. These are P-Channel enhancement mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17541.

Ordering Information

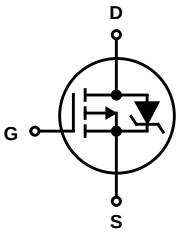
PART NUMBER	PACKAGE	BRAND
IRFR9110	TO-252AA	IF9110
IRFU9110	TO-251AA	IF9110

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., IRFR91109A.

Features

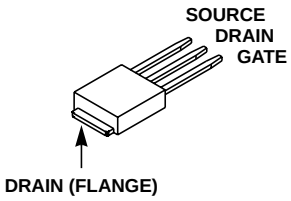
- 3.1A, 100V
- $r_{DS(ON)} = 1.200\Omega$
- Temperature Compensating PSPICE™ Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

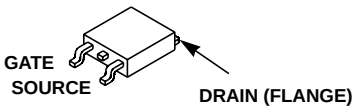


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.
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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRFR9110, IRFU9110	UNITS
Drain to Source Voltage	V_{DSS}	-100	V
Drain to Gate Voltage	V_{DGR}	-100	V
Gate to Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	3.1	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	25	W
Linear Derating Factor		0.2	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V		-100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100V, V_{GS} = 0V	$T_C = 25^oC$	-	-	-1	µA
			$T_C = 150^oC$	-	-	-50	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 1.9A, V_{GS} = -10V		-	-	1.200	Ω
Turn-On Time	t_{ON}	V_{DD} = -50V, I_D = 4A, R_L = 11Ω, V_{GS} = -10V, R_{GS} = 24Ω		-	-	50	ns
Turn-On Delay Time	$t_{d(ON)}$			-	10	-	ns
Rise Time	t_r			-	27	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	15	-	ns
Fall Time	t_f			-	17	-	ns
Turn-Off Time	t_{OFF}			-	-	50	ns
Total Gate Charge	Q_g	V_{GS} = 0 to -10V	V_{DD} = -80V, I_D = 3.1A, R_L = 25.8Ω	-	-	8.7	nC
Gate to Drain Charge	Q_{gd}			-	-	4.1	nC
Gate to Source Charge	Q_{gs}			-	-	2.2	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz		-	290	-	pF
Output Capacitance	C_{OSS}			-	94	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	18	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	5.00	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	100	$^oC/W$

Source to Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = -3.1A	-	-	-5.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = -4.0A, dI_{SD}/dt = -100A/µs	-	105	160	ns
Reverse Recovery Charge	Q_{RR}			0.51	1.0	µC

Typical Performance Curves Unless Otherwise Specified

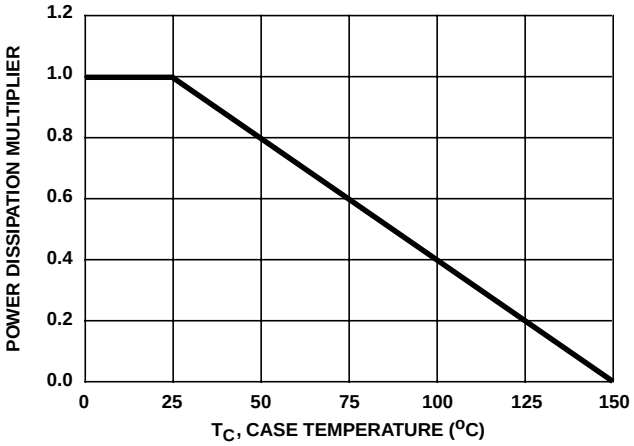


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

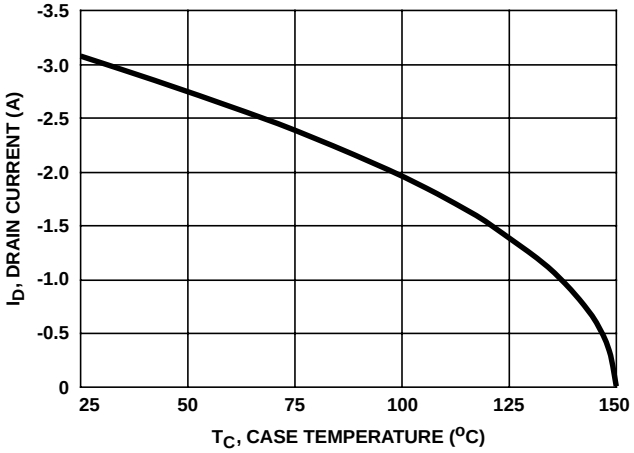


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

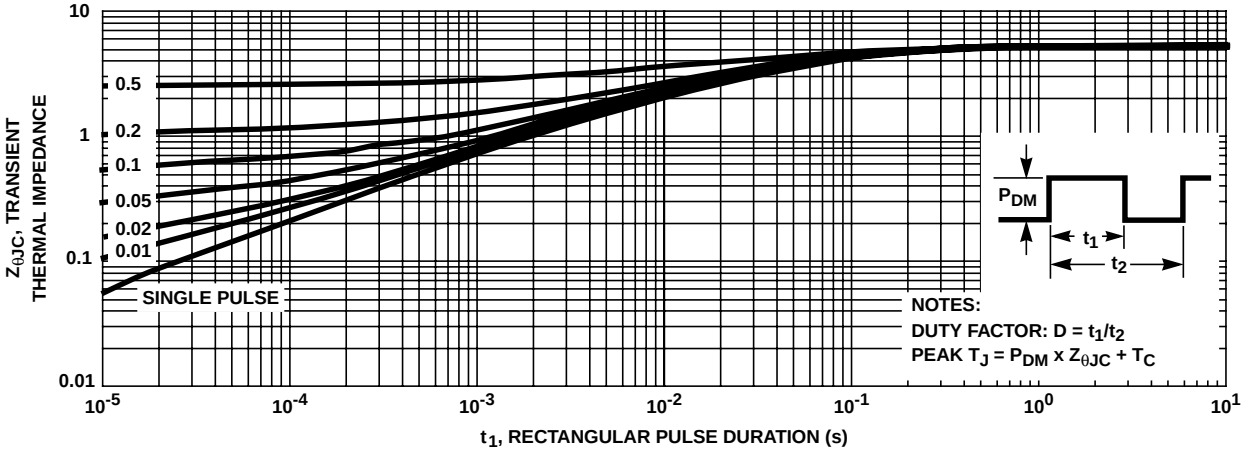


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

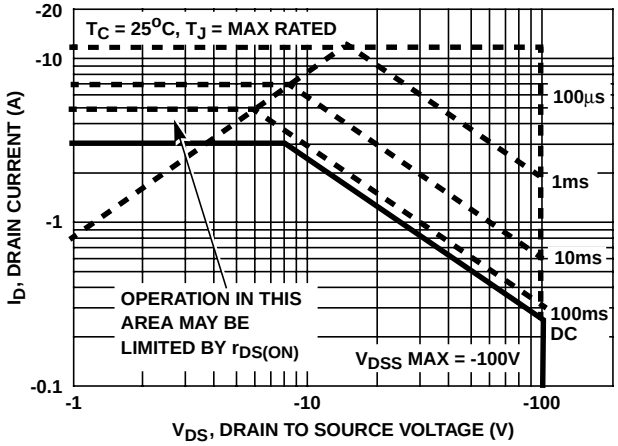


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

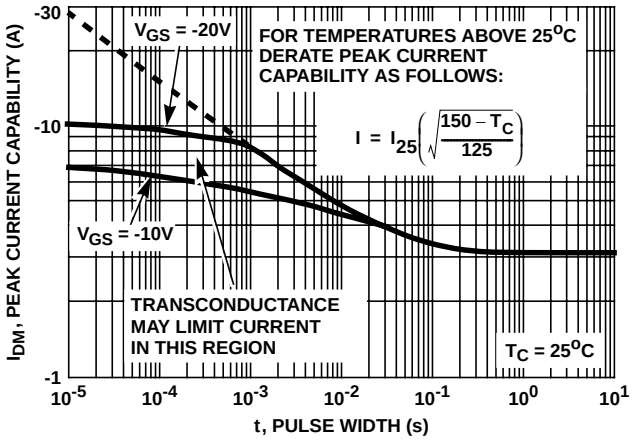


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)

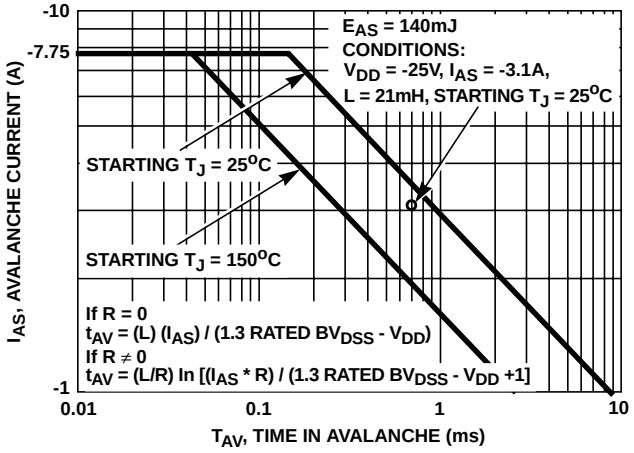


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

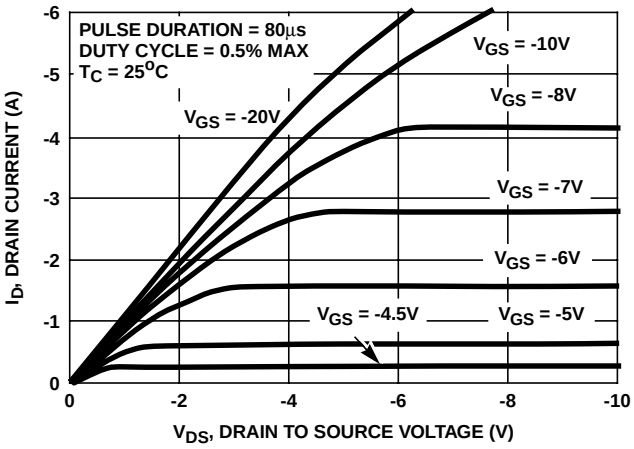


FIGURE 7. SATURATION CHARACTERISTICS

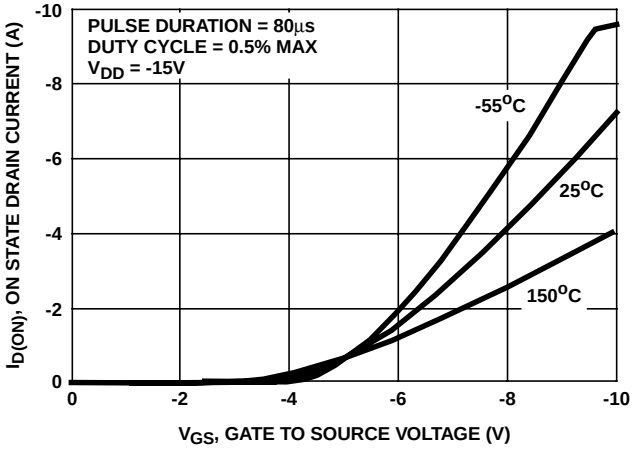


FIGURE 8. TRANSFER CHARACTERISTICS

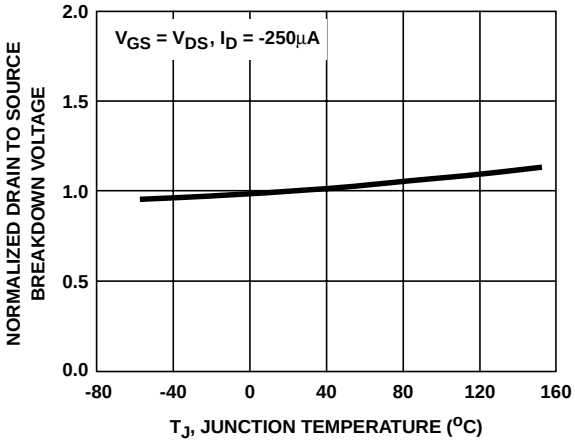


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

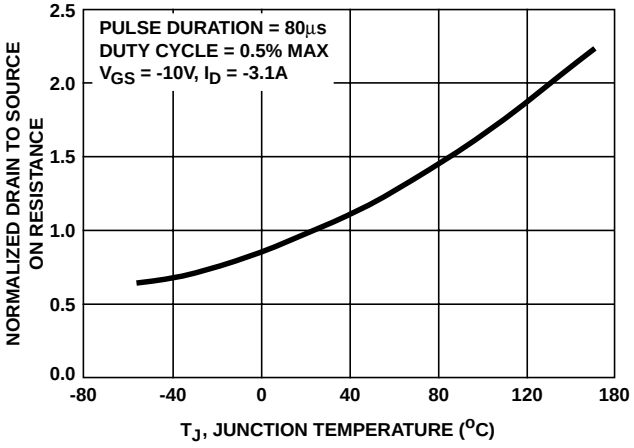


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

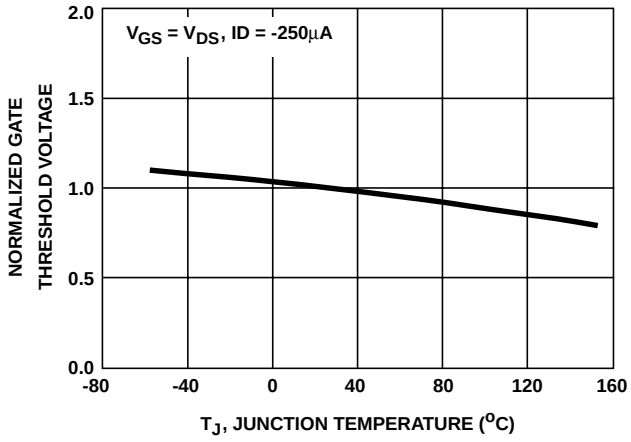


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

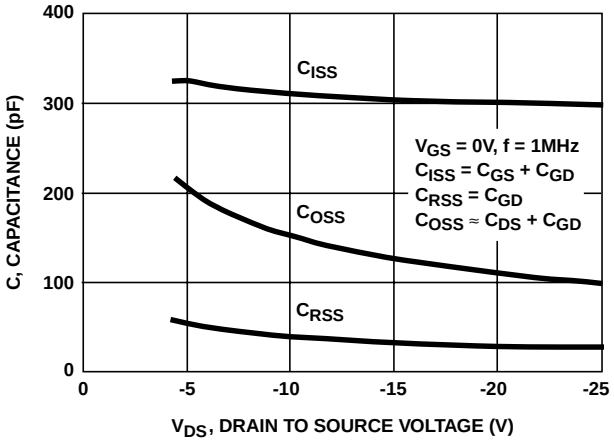
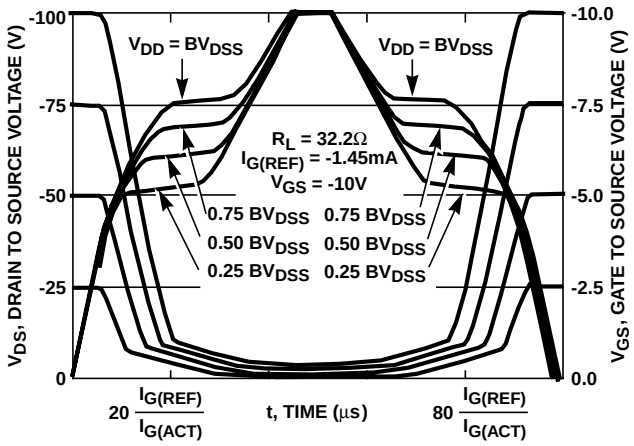


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

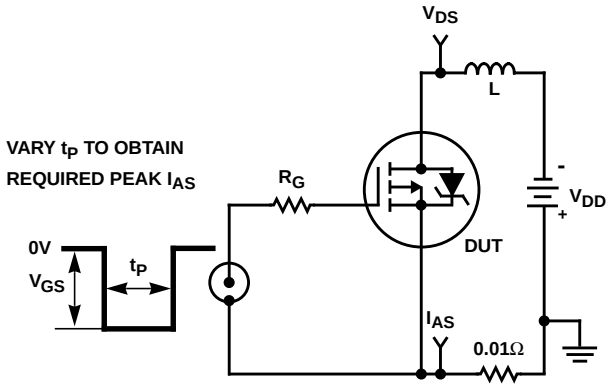


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

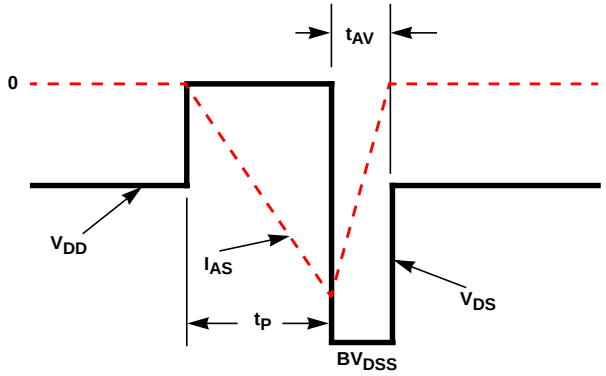


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

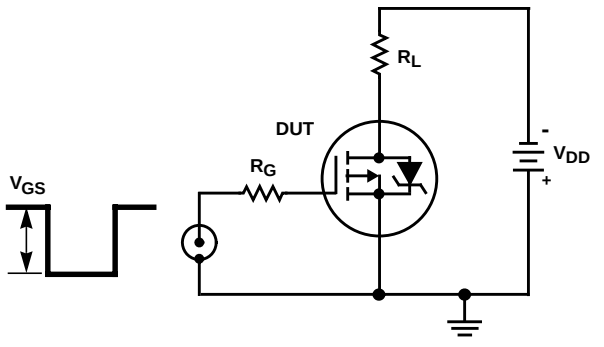


FIGURE 16. SWITCHING TIME TEST CIRCUIT

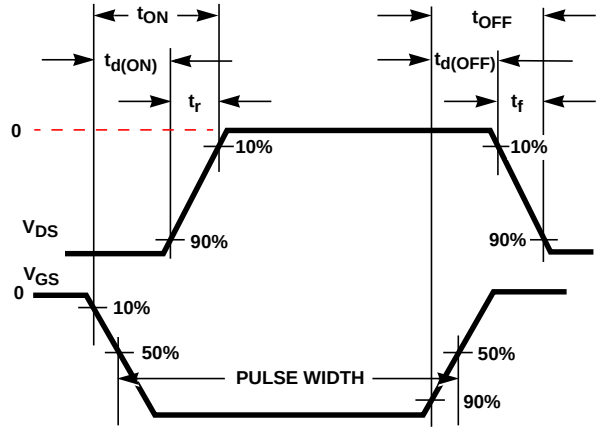


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

```
.SUBCKT IRFU9220  2  1  3        REV 9/6/94

CA 12 8 723e-12
CB 15 14 733e-12
CIN 6 8 517e-12

DBODY 5  7  DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 7 11 17 18  -244.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.609e-9
LSOURCE 3 7 2.609e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 1.194
RGATE 9 20 2.17
RIN 6 8 1e9
RLDRAIN 2 5 10
RLGATE 1 9 26.09
RLSOURCE 3 7 26.09
RSCL1  5  51  RSCLMOD  1e-6
RSCL2  5  50  1e3
RSOURCE 8 7 RDSMOD 90.1e-3
RVTO 18 19 RVTOMOD 1

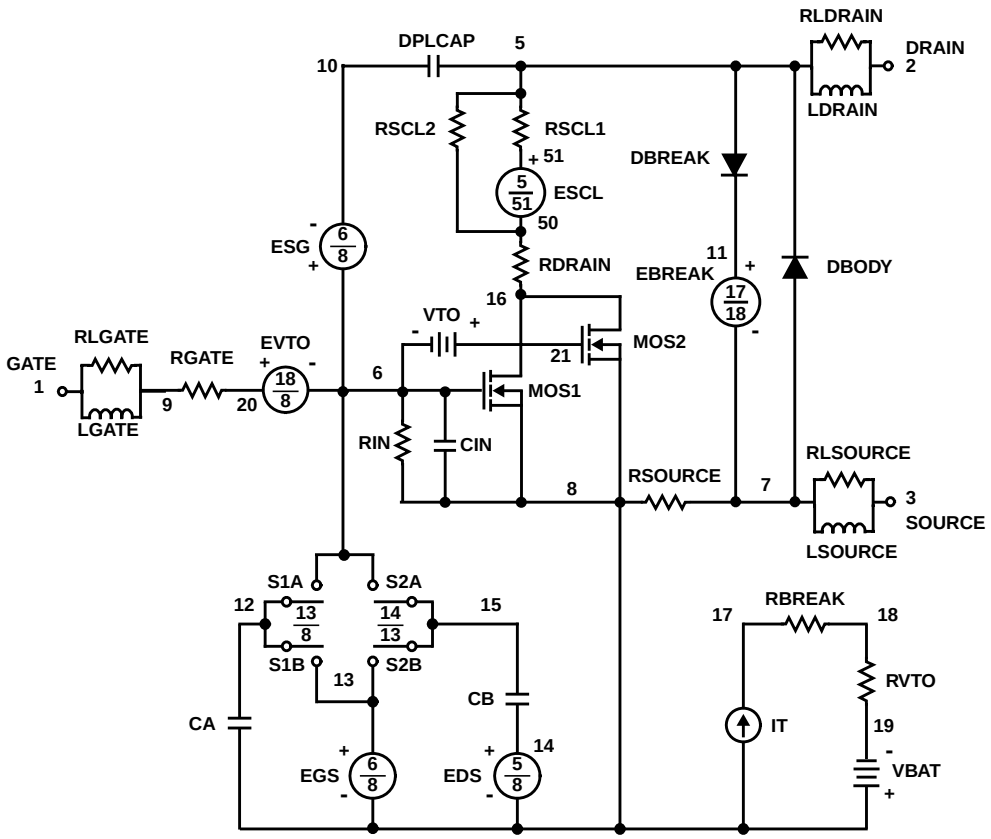
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.77

ESCL  51  50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/4.6,6))}

.MODEL DBDMOD D (IS=2.56e-14 RS=8.09e-2 TRS1=-2.45e-3 TRS2=-1.33e-5 CJO=4.21e-10 TT=1.17e-7)
.MODEL DBKMOD D (RS=5.07 TRS1=-1.05e-3 TRS2=1.28e-5)
.MODEL DPLCAPMOD D (CJO=170e-12 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.58 KP=1.38 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=1.1e-3 TC2=-2.73e-6)
.MODEL RDSMOD RES (TC1=6.95e-3 TC2=2.23e-5)
.MODEL RSCLMOD  RES (TC1=2.40e-3  TC2=-1.5e-5)
.MODEL RVTOMOD RES (TC1=-3.27e-3 TC2=-1.33e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=5.29 VOFF=3.29)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.29 VOFF=5.29)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.1 VOFF=-4.9)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.9 VOFF=0.1)


.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

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